Standards Manager Web Standards List

VITA-VMEbus International Trade Association

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1	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2024	VITA	
2	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2024	VITA	
3	87.0	High Density (HD) MT Circular Connector - Type 1	2024	VITA	
4	91.0	Connector for Higher Density VPX Applications	2024	VITA	
5	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2023	VITA	
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7	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By Cooling Technology	2023	VITA	0
8	62.1	Three Phase High-Voltage Power Supply Front- End in a 3U Plug-In Module Standard	2023	VITA	0
9	65.0	OpenVPX System Standard	2023	VITA	0
10	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2023	VITA	0
11	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2023	VITA	
12	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2022	VITA	
13	46.11	System Management on VPX	2022	VITA	293
14	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2022	VITA	20
15	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2022	VITA	60
16	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2022	VITA	59
17	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2022	VITA	54
18	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2022	VITA	36
19	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2022	VITA	102
20	66.5	Optical Interconnect on VPX - Hybrid Variants	2022	VITA	84
21	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2022	VITA	77
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23	78.00	SpaceVPX Systems	2022	VITA	624
24	88.0	Switched Mezzanine Card Plus (XMC+) Standard	2021	VITA	44
25	76.0	High Performance Cable Standard - Ruggedized 10 Gbaud Bulkhead Connector for Cu and AOC Cables	2021	VITA	60
26	42.0	XMC	2021	VITA	83
27	65.0	OpenVPX System Standard	2021	VITA	921
28	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2021	VITA	80
29	68.2	VPX Standard S-Parameter Definition	2021	VITA	28

30	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2020	VITA	28
31	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2020	VITA	28
32	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2020	VITA	70
33	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2020	VITA	70
34	62.2	This standard provides requirements for building a 270 volt/3U or 6U class power supply module that can be used to power a VPX chassis in the VITA 62 family of standards in high altitude applications.	2020	VITA	47
35	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2020	VITA	38
36	46.30	Higher Data Rate VPX	2020	VITA	30
37	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2020	VITA	16
38	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2020	VITA	47
39	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2020	VITA	54
40	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2020	VITA	40
41	62.2	This standard provides requirements for building a 270 volt/3U or 6U class power supply module that can be used to power a VPX chassis in the VITA 62 family of standards in high altitude applications.	2020	VITA	47
42	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2020	VITA	38
43	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2020	VITA	40
44	46.30	Higher Data Rate VPX	2020	VITA	30
45	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2020	VITA	16
46	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2020	VITA	47
47	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2020	VITA	54
48	46.31	Higher Data Rate VPX, Solder Tail	2020	VITA	30
49	46.31	Higher Data Rate VPX, Solder Tail	2020	VITA	31
50	65.0	OpenVPX System Standard	2019	VITA	868
51	47.0	Construction, Safety, and Quality for Plug-In Modules Standard	2019	VITA	26
52	47.1	Common Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard.	2019	VITA	35
53	47.2	Class 2 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	18
54	47.3	Class 3 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	19
55	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	121
56	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	122
57	65.0	OpenVPX System Standard	2019	VITA	868

58	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2019	VITA	80
59	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2019	VITA	64
60	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2019	VITA	26
61	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2019	VITA	25
62	86	High Voltage Input Sealed Connector Power Supply	2019	VITA	22
63	47.0	Construction, Safety, and Quality for Plug-In Modules Standard	2019	VITA	26
64	47.1	Common Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard.	2019	VITA	35
65	47.2	Class 2 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	18
66	47.3	Class 3 Requirements for Environments, Design and Construction, Safety, and Quality for VITA 47 Plug-In Modules Dot Standard	2019	VITA	19
67	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2019	VITA	122
68	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0].	2019	VITA	13
69	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2019	VITA	81
70	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2019	VITA	26
71	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2019	VITA	27
72	86	High Voltage Input Sealed Connector Power Supply	2019	VITA	22
73	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant â__The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	15
74	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant â__The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	16
75	57.4	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	67
76	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2018	VITA	28
77	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2018	VITA	34
78	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2018	VITA	45
79	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2018	VITA	31
80	46.3	Serial RapidIO__ on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2018	VITA	47
81	46.4	PCI Express¦_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express¦_ Fabric in the VITA46 environment and to define the mapping of the PCI Express¦ Links on the VPX connector.	2018	VITA	21

82	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2018	VITA	32
83	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2018	VITA	27
84	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2018	VITA	92
85	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2018	VITA	58
86	41.1	VXS 4X InfiniBandâ__ Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2018	VITA	24
87	41.2	VXS 4X Serial RapidIOâ__ Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2018	VITA	25
88	42.1	XMC Switched Mezzanine Card: Parallel RapidIOâ__ 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2018	VITA	30
89	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2018	VITA	15
90	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2018	VITA	53
91	17.3	Serial Front Panel Data Port (sFPDP) Gen 3.0	2018	VITA	54
92	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2018	VITA	19
93	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	15
94	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2018	VITA	16
95	57.4 ERTA	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	73
96	57.4	This standard extends the VITA 57.1 FMC standard by specifying two new connectors that enable additional Gigabit Transceiver interfaces that run at up to 28Gbps. It also describes FMC+ IO modules which support this enhanced version of the FMC electro-mech	2018	VITA	67
97	42.1	XMC Switched Mezzanine Card: Parallel RapidIO 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2018	VITA	30
98	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2018	VITA	15
99	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2018	VITA	33
100	46.3	Serial RapidIO on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2018	VITA	47
101	46.4	PCI Expressî_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Expressî_ Fabric in the VITA46 environment and to define the mapping of the PCI Expressî Links on the VPX connector.	2018	VITA	21
102	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2018	VITA	32
103	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2018	VITA	27
104	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2018	VITA	92

105	48.4	This standard establishes the mechanical design interface control, outline and mounting requirements for a liquid-flow-through cooled Plug-In Module to ensure the mechanical intermateability of 6U VPX liquid-flow-through cooled Plug-In Module within assoc	2018	VITA	53
106	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2018	VITA	28
107	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2018	VITA	34
108	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2018	VITA	60
109	41.1	VXS 4X InfiniBand Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2018	VITA	26
110	41.2	VXS 4X Serial RapidIO Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2018	VITA	25
111	17.3	Serial Front Panel Data Port (sFPDP) Gen 3.0	2018	VITA	54
112	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2018	VITA	19
113	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2017	VITA	50
114	49.02	VITA Radio Transport (VRT) Standard for Electromagnetic Spectrum: Signals and Applications	2017	VITA	361
115	49.2	The ANSI/VITA 49.2 standard, which is part of the VITA Radio Transport (VRT) family of standards, defines a signal/spectrum protocol that expresses spectrum observation, spectrum operations, and capabilities of RF devices. This is done independent of manu	2017	VITA	359
116	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2017	VITA	33
117	53.0	Standard for Commercial Technology Market Surveillance This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2017	VITA	24
118	65.1	This standard documents variations of Slot, Backplane, and Modules Profiles. As part of the Slot Profile Description, there are also some Connector Modules defined. This document is primarily tables which are referenced by [VITA 65.0]. PDF Version.	2017	VITA	58
119	65.0	OpenVPX System Standard	2017	VITA	769
120	68.1	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	46
121	67.3	Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane	2017	VITA	41
122	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2017	VITA	25
123	68.1 ERTA	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	49
124	74.0	Compliant System Small Form Factor Module Base Standard	2017	VITA	92
125	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2017	VITA	32
126	49.2	The ANSI/VITA 49.2 standard, which is part of the VITA Radio Transport (VRT) family of standards, defines a signal/spectrum protocol that expresses spectrum observation, spectrum operations, and capabilities of RF devices. This is done independent of manu	2017	VITA	359
127	48.8	Mechanical Standard for Electronic VPX Plug-in Modules Using Air Flow Through Cooling	2017	VITA	50
128	53.0	Standard for Commercial Technology Market Surveillance â__ This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2017	VITA	24
129	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2017	VITA	24
130	68.1 ERTA	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2017	VITA	51

131	74.0	Compliant System Small Form Factor Module Base Standard	2017	VITA	92
132	66.4	Optical Interconnect On VPX - Half Width MT Variant	2016	VITA	19
133	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2016	VITA	22
134	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2016	VITA	97
135	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2016	VITA	46
136	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2016	VITA	21
137	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2016	VITA	36
138	42.0	XMC	2016	VITA	44
139	68.1	VPX Compliance Channel - Fixed Signal Integrity Budget Standard	2016	VITA	47
140	68.0	VITA 68.0 is the Base Standard of the VITA 68.x family of standards for signal integrity compliance of VPX systems and components.	2016	VITA	26
141	76.0	High Performance Cable Standard - Ruggedized 10 Gbaud Bulkhead Connector for Cu and AOC Cables	2016	VITA	61
142	78.00 ERTA	SpaceVPX Systems	2016	VITA	410
143	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2016	VITA	22
144	66.4	Optical Interconnect On VPX - Half Width MT Variant	2016	VITA	19
145	67.1 ERTA	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2016	VITA	24
146	62	Modular Power Supply Standard	2016	VITA	97
147	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2016	VITA	45
148	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2016	VITA	46
149	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2016	VITA	21
150	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2016	VITA	36
151	42.0	XMC	2016	VITA	44
152	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2015	VITA	17
153	49A	Spectrum Survey Interoperability Specification	2015	VITA	44
154	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2015	VITA	184
155	46.10	Rear Transition Module for VPX	2015	VITA	38
156	46.11	System Management on VPX	2015	VITA	228

157	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2015	VITA	42
158	63.0	Hyperboloid Alternative Connector for VPX	2015	VITA	43
159	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2015	VITA	18
160	78.00	SpaceVPX Systems	2015	VITA	404
161	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines â__Serial FPDPâ__, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2015	VITA	42
162	46.10	Rear Transition Module for VPX	2015	VITA	38
163	46.11	System Management on VPX	2015	VITA	228
164	49A	Spectrum Survey Interoperability Specification	2015	VITA	44
165	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2015	VITA	184
166	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2015	VITA	18
167	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2015	VITA	17
168	63.0	Hyperboloid Alternative Connector for VPX	2015	VITA	43
169	78.00	SpaceVPX Systems	2015	VITA	410
170	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2014	VITA	25
171	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2014	VITA	27
172	39	PCI-X for PMC and Processor PMC - This standard integrates the PCI-X capability from PCI to PMC based products, including standard PMCs as well as Processor PMCs.	2014	VITA	11
173	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By__Cooling Technology	2014	VITA	37
174	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2014	VITA	34
175	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2014	VITA	17
176	32	Processor PMC - This standard incorporates a set of extensions to the IEEE 1386.1 PMC (__PCI Mezzanine Card__) standard which creates a new class of CPU based PMC cards referred to in this standard as Processor PMC cards.	2014	VITA	15
177	1.7	Increased Current DIN Connector- This standard describes increased current levels, test methods, test data and compliance criteria for 3 row DIN and 5 row DIN connectors when used in VME, VME64 and VME64 Extension P1/J1 and P2/J2 pin out arrangements.	2014	VITA	11
178	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second	2014	VITA	48
179	61.0	XMC 2.0 - This standard, based upon VITA 42.0 XMC, defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed form factor, but utilizing an alternate, ruggedized, high speed mezzanine interconnector	2014	VITA	25
180	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2014	VITA	27
181	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2014	VITA	35
182	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2014	VITA	17
183	32	Processor PMC - This standard incorporates a set of extensions to the IEEE 1386.1 PMC (__PCI Mezzanine Card__) standard which creates a new class of CPU based PMC cards referred to in this standard as Processor PMC cards.	2014	VITA	15

184	39	PCI-X for PMC and Processor PMC - This standard integrates the PCI-X capability from PCI to PMC based products, including standard PMCs as well as Processor PMCs.	2014	VITA	11
185	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second	2014	VITA	48
186	1.7	Increased Current DIN Connector- This standard describes increased current levels, test methods, test data and compliance criteria for 3 row DIN and 5 row DIN connectors when used in VME, VME64 and VME64 Extension P1/J1 and P2/J2 pin out arrangements.	2014	VITA	11
187	48.7	Mechanical Standard for Electronic Plug-in units using Air Flow-By__Cooling Technology	2014	VITA	37
188	42.0	XMC	2014	VITA	40
189	42.3	XMC PCI Express Protocol Layer Standard - This standard defines the implementation of PCI Express on VITA 42.0, XMC.	2014	VITA	37
190	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2013	VITA	109
191	46.1	Rear Transition Module for VPX - This standard defines a rear transition module (RTM) for VPX applications.	2013	VITA	33
192	46.9 ERTA	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2013	VITA	71
193	46.6	Gigabit Ethernet Control Plane on VPX - The objectives of this standard are to assign Gigabit Ethernet Port mappings for the purpose of Control Plane communication onto the VPX connectors for both 3U and 6U form factors and to provide rules and recommenda	2013	VITA	32
194	46.11	System Management on VPX	2013	VITA	208
195	51.1	Reliability Prediction MIL-HDBK-217 Subsidiary Specification	2013	VITA	34
196	38	Describes a methodology for using IPMI for System Management of VME systems.	2013	VITA	18
197	58.1	Line Replaceable Integrated Electronics Chassis Standard, Liquid Cooled Chassis - The objective of this standard is to identify the particular requirements for a chassis configuration conforming to the ANSI/VITA 58.0 base standard.	2013	VITA	27
198	66.2	Optical Interconnect On VPX - ARINC 801 Termini Variant The VITA 66.2 standard defines an ARINC 801 Termini Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2013	VITA	15
199	73.0	VITA 73.0 Rugged Small Form Factor - This document provides mechanical and electrical guidelines for the standardization of switched serial interconnects in small form-factor applications, with specific concern taken to allow deployment in ruggedized envi	2013	VITA	54
200	74.0	Compliant System Small Form Factor Module Base Standard	2013	VITA	67
201	38	Describes a methodology for using IPMI for System Management of VME systems.	2013	VITA	16
202	58.1	Line Replaceable Integrated Electronics Chassis Standard, Liquid Cooled Chassis - The objective of this standard is to identify the particular requirements for a chassis configuration conforming to the ANSI/VITA 58.0 base standard.	2013	VITA	27
203	73.0	VITA 73.0 Rugged Small Form Factor - This document provides mechanical and electrical guidelines for the standardization of switched serial interconnects in small form-factor applications, with specific concern taken to allow deployment in ruggedized envi	2013	VITA	54
204	75.0	VITA 75 Rugged Small Form Factor - This draft standard for a rugged small form factor describes overall subsystem attributes such as the envelope of the subsystem box and the organization of the dot specifications.	2012	VITA	23
205	75.11	This draft standard provides requirements for front panels, connectors, signal pin assignments, and power for VITA 75 subsystems.	2012	VITA	142
206	75.20	Rugged Small Form Factor ù Cooled via Free Air Convection	2012	VITA	26
207	75.22	This draft standard standardizes mounting and cooling for conduction to a cold plate cooled VITA 75 subsystems.	2012	VITA	20
208	66.1	Optical Interconnect On VPX - MT Variant â__The VITA 66.1 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2012	VITA	14
209	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	2012	VITA	42
210	75.0	VITA 75 Rugged Small Form Factor - This draft standard for a rugged small form factor describes overall subsystem attributes such as the envelope of the subsystem box and the organization of the dot specifications.	2012	VITA	22

211	75.11	This draft standard provides requirements for front panels, connectors, signal pin assignments, and power for VITA 75 subsystems.	2012	VITA	141
212	75.20	Rugged Small Form Factor ù Cooled via Free Air Convection	2012	VITA	25
213	75.22	This draft standard standardizes mounting and cooling for conduction to a cold plate cooled VITA 75 subsystems.	2012	VITA	19
214	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	2012	VITA	60
215	65	The OpenVPX System Specification was created to bring versatile system architectural solutions to the VPX market. Based on the extremely flexible VPX family of standards, the OpenVPX standard uses module mechanical, connectors, thermal, communications pro	2012	VITA	555
216	67.1	Coaxial Interconnect on VPX, 3U, 4 Position, SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a 3U VITA 46 interface containing multi-position blind mate analog	2012	VITA	23
217	67.2	Coaxial Interconnect on VPX, 8 Position SMPM Configuration - The objective of this standard is to detail the configuration and interconnect within the structure of VITA 67.0 enabling a VITA 46 interface containing multi-position blind mate analog connecto	2012	VITA	24
218	67.0	Coaxial Interconnect on VPX - Base Standard - The objective of this standard is to establish a structure for implementing blind mate analog coaxial interconnects with VPX backplanes and plug-in modules, and to define a specific family of interconnects and	2012	VITA	25
219	66.3	Optical Interconnect On VPX - Mini-Expanded Beam Variant The VITA 66.3 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2012	VITA	16
220	60.0	Alternative Connector for VPX - This standard provides an alternate connector to the one specified in the VITA 46.0 VPX Baseline Standard. Because the 46.0 and the 60.0 connectors are not intermateable, a VITA 60.0 module will not plug into a VITA 46.0.0	2012	VITA	45
221	62.0	VPX: Modular Power Supply - This standard provides a set of requirements for power supply modules that can be used in VPX systems.	2012	VITA	91
222	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	2012	VITA	44
223	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	2012	VITA	62
224	51.0	Reliability Prediction - This document provides an electronics failure rate prediction standard, and establishes a Community of Practice. It addresses the limitations of existing prediction practices with a series of subsidiary specifications that contain	2012	VITA	28
225	46.3	Serial RapidIO on VPX Fabric Connector - This standard assigns Serial RapidIO ports to the VPX P1/J1 connector.	2012	VITA	47
226	46.4	PCI Express¦_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express¦_ Fabric in the VITA46 environment and to define the mapping of the PCI Express¦ Links on the VPX connector.	2012	VITA	21
227	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2012	VITA	27
228	42.2	XMC Serial RapidIO Protocol Layer Standard - This standard defines the implementation of Serial RIO on VITA 42.0, XMC.	2012	VITA	17
229	42.1	XMC Switched Mezzanine Card: Parallel RapidIO 8/16 LP-LVDS Protocol Layer Standard - This standard defines the implementation of Parallel RIO on VITA 42.0, XMC.	2012	VITA	32
230	46.8	InfiniBand on VPX Fabric Connector - The objectives of this draft standard are to assign InfiniBand ports to the VPX connectors and to provide rules and recommendations for the use of the assigned InfiniBand ports.	2011	VITA	52
231	51.2	Physics of Failure Reliability Predictions - This specification provides standard processes, instructions and default parameters for using the Physics of Failure (PoF) approach for modeling the reliability of electronic products. It includes a discussion	2011	VITA	57
232	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	2011	VITA	55
233	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	2011	VITA	15
234	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	2011	VITA	97

235	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	2011	VITA	72
236	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	2011	VITA	33
237	1.6	Keying for Conduction Cooled VME64x.	2011	VITA	29
238	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	2011	VITA	305
239	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	2011	VITA	66
240	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2011	VITA	100
241	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework.	2011	VITA	48
242	35	Provides pin assignments for PMC P4 connector to VME P0 and P2 connectors.	2011	VITA	18
243	30	2mm Connector Practice for Euroboard Systems - This standards provides the dimensions for Euroboard systems that use 2mm connectors.	2011	VITA	37
244	41.2	VXS 4X Serial RapidIO Protocol Layer Standard - This standard describes a method for implementing Serial Rapid I/O on ANSI/VITA 41.0, VXS.	2011	VITA	27
245	20	CCPMC - Conduction Cooled PMC - This standard defines the mechanical requirements for compliance with conduction cooled PMC modules.	2011	VITA	21
246	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	2011	VITA	46
247	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	2011	VITA	123
248	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	2011	VITA	52
249	66.0	Optical Interconnect on VPX - Base Standard -- The VITA 66.0 base standard defines physical features of a stand-alone compliant blind mate Optical Interconnect for use in VPX systems.	2011	VITA	19
250	66.1	Optical Interconnect On VPX - MT Variant The VITA 66.1 standard defines an MT Variant blind mate fiber optic interconnect for use with VPX backplanes and plug-in modules.	2011	VITA	14
251	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	2011	VITA	46
252	1.6	Keying for Conduction Cooled VME64x.	2011	VITA	27
253	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	2011	VITA	64
254	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	2011	VITA	95
255	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	2011	VITA	13
256	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	2011	VITA	72
257	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	2011	VITA	53
258	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	2011	VITA	31
259	35	Provides pin assignments for PMC P4 connector to VME P0 and P2 connectors.	2011	VITA	16
260	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	2011	VITA	123
261	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	2011	VITA	52
262	30	2mm Connector Practice for Euroboard Systems - This standards provides the dimensions for Euroboard systems that use 2mm connectors.	2011	VITA	35

263	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	2011	VITA	303
264	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2011	VITA	100
265	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework	2011	VITA	48
266	46.8	InfiniBand on VPX Fabric Connector - The objectives of this draft standard are to assign InfiniBand ports to the VPX connectors and to provide rules and recommendations for the use of the assigned InfiniBand ports.	2011	VITA	51
267	65	The OpenVPX System Specification was created to bring versatile system architectural solutions to the VPX market. Based on the extremely flexible VPX family of standards, the OpenVPX standard uses module mechanical, connectors, thermal, communications pro	2010	VITA	555
268	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2010	VITA	82
269	53.0	Standard for Commercial Technology Market Surveillance This standard describes the types of market surveillance data needed by Department of Defense program managers in order to develop and implement technology refresh plans.	2010	VITA	24
270	51.3	Qualification and Environmental Stress Screening in Support of Reliability Predictions - This standard provides rules, permissions, and observations to assure that cost effective Qualification and Environmental Stress Screening support valid reliability p	2010	VITA	21
271	48.0	Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)	2010	VITA	17
272	48.5	Establishes the design requirements for an air-flow-through cooled plug-in unit with a form factor as close to 6U as possible while retaining the VITA 46 connector layout. Unlike ANSI/VITA 48.1, which uses cooling air impinged directly upon the components	2010	VITA	33
273	48.2	This Standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	2010	VITA	53
274	48.1	This standard defines the mechanical requirements that are needed to insure the mechanical interchangeability of air cooled 3U and 6U Plug-In Modules and define the features required to achieve Two Level Maintenance compatibility.	2010	VITA	48
275	46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard - This VITA 46 (VPX) subsidiary standard defines PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	2010	VITA	70
276	46.4	PCI Express¦_ on the VPX Fabric Connector - The objective of this standard is the implementation of the PCI Express¦_ Fabric in the VITA46 environment and to define the mapping of the PCI Express¦ Links on the VPX connector.	2010	VITA	17
277	46.10	Rear Transition Module for VPX	2009	VITA	38
278	42.6	XMC 10 Gigabit Ethernet 4-Lane Protocol Layer Standard - This standard defines a method for supporting 10 Gigabit Ethernet using XAUI switched interconnect protocol on the XMC form factor.	2009	VITA	19
279	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2009	VITA	17
280	49.1	This standard specifies an optional encapsulation protocol for VITA-49.0 (VRT) packets.	2009	VITA	18
281	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2009	VITA	179
282	49.0	The VITA Radio Transport (VRT) standard defines a transport-layer protocol designed to promote interoperability between RF (radio frequency) receivers and signal processing equipment in a wide range of applications.	2009	VITA	184
283	41.6	VXS 1X Gbit Ethernet - This standard describes a method for implementing Ethernet as a control channel on ANSI/VITA 41.0, VXS.	2009	VITA	35
284	41.6	VXS 1X Gigabit Ethernet Control Channel Layer Standard	2009	VITA	32
285	31.1	Gigabit Ethernet on VME64x Backplanes - This standard defines a pin assignment and interconnection methodology for implementing a 10/100/1000BASE-T Ethernet switched network on a ANSI/VITA 1.1 VME64x backplane.	2009	VITA	18
286	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2009	VITA	43
287	58.0	This standard provides common design and performance requirements for a family of integrated electronic chassis incorporating updated industry standard high speed electronic assemblies and designed for rugged environments.	2009	VITA	27

288	57.1	FPGA Mezzanine Card (FMC) Standard - This standard defines the mechanical format and signal assignments for an FPGA mezzanine card interface.	2008	VITA	79
289	30.1	2mm Connector Practice for Conduction Cooled Euroboard Systems - This standard defines the dimensions for conduction cooled Euroboards when used with 2mm connectors.	2008	VITA	37
290	42.0	XMC	2008	VITA	40
291	46.7	Ethernet on VPX Fabric Connector - The objectives of this standard are to assign backplane Ethernet links to the VPX P1/J1 connector and to provide rules and recommendations for the use of Ethernet over backplane media.	2008	VITA	21
292	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2007	VITA	109
293	46.0	VPX Baseline Standard - This standard defines requirements for VPX.	2007	VITA	107
294	47	This standard defines environmental, design and construction, safety, and quality requirements for commercial-off-the-shelf (COTS) plug-in units (cards, modules, etc.) intended for mobile applications.	2007	VITA	22
295	41.1	VXS 4X InfiniBand Protocol Layer Standard - This standard describes a method for using the InfiniBand protocol on ANSI/VITA 41.0, VXS.	2006	VITA	26
296	41.0	VXS VMEbus Switched Serial Standard - This standard defines a method for using switched serial fabrics within the VMEbus framework.	2006	VITA	60
297	13	VMEbus Pin Assignment Standard for ISO/IEC 14575 (IEEE Std. 1355-1995 (H.I.C.)) - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only.	2006	VITA	14
298	19.1	BusNet Media Access Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the media access control layer for the BusNet backplane software protocol.	2006	VITA	64
299	19.2	BusNet Link Layer Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the link layer control layer for the Busnet backplane software protocol.	2006	VITA	18
300	25	VISION - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines a software application interface for VMEbus modules.	2006	VITA	135
301	29	PC.MIP - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the mechanical form factor and the pin assignments for a small form factor mezzanine module based on the PCI bus.	2006	VITA	66
302	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2003	VITA	40
303	17.1	Serial Front Panel Data Port (sFPDP) - This standard defines Serial FPDP, a high-speed low-latency serial communications protocol for use in high-speed data transfer applications, typically using a fiber optic link.	2003	VITA	42
304	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework.	2003	VITA	48
305	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	2003	VITA	100
306	40	Service and Status Indicator Standard. This standard defines the colors, behaviors, placement, and labeling of service indicator lamps for boards, field replaceable units, and enclosures.	2002	VITA	37
307	29	PC.MIP - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the mechanical form factor and the pin assignments for a small form factor mezzanine module based on the PCI bus.	2001	VITA	68
308	1.5	2eSST - This standard defines a new VME protocol that allows data transfers of up to 320 Mbytes/second. Reaffirmed in 2009. Stabilized in 2014.	1999	VITA	51
309	5.1	RACEway Interlink - This standard defines a high speed circuit switched point to point interconnect for use between VMEbus modules via the P2 connector.	1999	VITA	74
310	1.4	VME64x Live Insertion System Requirements	1998	VITA	29
311	26	Myrinet - This standard defines a packet switched interconnect protocol for implementation in a VMEbus environment.	1998	VITA	54
312	23	VME64 Extensions for Physics - This standard defines a series of recommended practices for the use of VMEbus in the physics community.	1998	VITA	125

313	17	Front Panel Data Port (FPDP) - This standard defines a point to point data interconnect for use on front panel Eurocard modules.	1998	VITA	48
314	19.1	BusNet Media Access Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the media access control layer for the BusNet backplane software protocol.	1998	VITA	66
315	19.2	BusNet Link Layer Control - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines the link layer control layer for the Busnet backplane software protocol.	1998	VITA	20
316	19.0	Summary and Introduction to the BusNet Standard	1997	VITA	19
317	25	VISION - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only. This standard defines a software application interface for VMEbus modules.	1997	VITA	137
318	1.1	VME64 Extensions - This standard covers extensions to the VME64 specification including the 160 pin connector, geographical addressing, and added power pins.	1997	VITA	98
319	1.3	VME64x 9U x 400 mm Format - This standard defines a 9U x 400 mm board layout for use within the VMEbus framework	1997	VITA	50
320	4.1	IP I/O Mapping to VME64x - This standard defines the pin assignments from IP Modules to the VME64x P0 and P2 connectors.	1996	VITA	15
321	6.1	SCSA Extensions - This standard provides feature extensions to the ANSI/VITA 6 standard.	1996	VITA	39
322	12	M-Module - This standard defines a mezzanine module specification for small sized printed circuit boards.	1996	VITA	63
323	10	SKYchannel - This standard was withdrawn as an American National Standard in 2012 and is provided for historical reference only. This standard defines a packet switched cross bar interconnect that runs on the VMEbus P2 connector.	1995	VITA	43
324	13	VMEbus Pin Assignment Standard for ISO/IEC 14575 (IEEE Std. 1355-1995 (H.I.C.)) - Historical Standard. This standard was withdrawn in 2006 and is provided for historical reference only.	1995	VITA	16
325	4	IP Module - This standard defines the requirements for a business card sized mezzanine module printed circuit board.	1995	VITA	97
326	3	Board Level Live Insertion - This standard defines several methodologies for using VMEbus modules in a live insertion framework.	1995	VITA	66
327	1	VME64 Standard - This standard covers the main body of the VMEbus specification. It includes both 32 bit and 64 bit usage.	1994	VITA	305
328	6	SCSA - This standard defines an isochronous backplane bus for telephony applications on the VMEbus P2 connector.	1994	VITA	55

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