Standards Manager Web Standards List

JEDEC-Joint Electron Device Engineering Council

Id	Number	Title	Year	Organization	Page
1	JEP106BG	STANDARD MANUFACTURERS IDENTIFICATION CODE	2023	JEDEC	
2	JEP114A	Guidelines for Particle Impact Noise Detection (PIND) Testing, Operator Training, and Certification	2023	JEDEC	
3	JEP130C	Guidelines for Packing and Labeling of Integrated Circuits in Unit Container Packing (Tubes, Trays, and Tape and Reel)	2023	JEDEC	
4	JEP142	GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID/MCM PRODUCTS	2023	JEDEC	
5	JEP146B	Guidelines for Supplier Performance Rating	2023	JEDEC	
6	JEP163A	SELECTION OF BURN-IN / LIFE TEST CONDITIONS AND CRITICAL PARAMETERS FOR QML MICROCIRCUITS	2023	JEDEC	
7	JEP166E	JC-42.6 MANUFACTURER IDENTIFICATION (ID) CODE FOR LOW POWER MEMORIES	2023	JEDEC	
8	JEP183A	Guidelines for Measuring the Threshold Voltage (VT) of SiC MOSFETs	2023	JEDEC	
9	JEP192	Guidelines for Gate Charge (QG) Test Method for SiC MOSFET	2023	JEDEC	
10	JEP193	Survey On Latch-Up Testing Practices and Recommendations for Improvements	2023	JEDEC	
11	JEP194	Guideline for Gate Oxide Reliability and Robustness Evaluation Procedures for Silicon Carbide Power MOSFETs	2023	JEDEC	
12	JEP195	Guideline for Evaluating Gate Switching Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion	2023	JEDEC	
13	JEP30-A100A	Part Model Assembly Process Classification Guidelines for Electronic-Device Packages XML Requirements	2023	JEDEC	
14	JEP30-E100B	Part Model Electrical Guidelines for Electronic-Device Packages XML Requirements	2023	JEDEC	
15	JEP30-P100B	Part Model Package Guidelines for Electronic-Device Packages XML Requirements	2023	JEDEC	
16	JEP30-S100	Part Model SupplyChain Guidelines for Electronic-Device Packages XML Requirements	2023	JEDEC	
17	JEP30-T100A	Part Model Thermal Guidelines for Electronic-Device Packages XML Requirements	2023	JEDEC	
18	JEP30B	Part Model Guidelines for Electronic-Device Packages XML Requirements	2023	JEDEC	
19	JESD15-1.01	COMPACT THERMAL MODEL OVERVIEW	2023	JEDEC	
20	JESD206.01	FBDIMM: ARCHITECTURE AND PROTOCOL	2023	JEDEC	
21	JESD207.01	RADIO FRONT END - BASEBAND DIGITAL PARALLEL (RBDP) INTERFACE	2023	JEDEC	
22	JESD22-A104F.01	Temperature Cycling	2023	JEDEC	
23	JESD230F.01	NAND Flash Interface Interoperability	2023	JEDEC	
24	JESD232A.01	GRAPHICS DOUBLE DATA RATE (GDDR5X) SGRAM STANDARD	2023	JEDEC	
25	JESD238A	HIGH BANDWIDTH MEMORY (HBM3) DRAM	2023	JEDEC	
26	JESD250D	Graphics Double Data Rate (GDDR6) SGRAM Standard	2023	JEDEC	
27	JESD282B.02	SILICON RECTIFIER DIODES:	2023	JEDEC	
28	JESD300-5B.01	SPD5118 HUB and SERIAL PRESENCE DETECT DEVICE STANDARD	2023	JEDEC	
29	JESD302-1A	TS511X, TS521X Serial Bus Thermal Sensor Device Standard	2023	JEDEC	
30	JESD30K	DESCRIPTIVE DESIGNATION SYSTEM FOR ELECTRONIC-DEVICE PACKAGES	2023	JEDEC	
31	JESD317	Compute Express Link (CXL) Memory Module Base Standard	2023	JEDEC	
32	JESD400-5A.01	DDR5 Serial Presence Detect (SPD) Contents	2023	JEDEC	
33	JESD401-5A	DDR5 DIMM Labels	2023	JEDEC	
34	JESD557D	Statistical Process Control Systems	2023	JEDEC	

35	JESD405-1	Compute Express Link (CXL) Memory Module Label	2023	JEDEC	
36	JESD82-12A.01	DEFINITION OF THE SSTU32S869 AND SSTU32D869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS	2023	JEDEC	
37	JESD82-13A.01	DEFINITION OF THE SSTVN16859 2.5-2.6 V 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR PC1600, PC2100, PC2700 AND PC3200 DDR DIMM APPLICATIONS	2023	JEDEC	
38	JESD82-17.01	DEFINITION OF THE SSTUA32S868 AND SSTUA32D868 REGISTERED BUFFER WITH PARITY FOR 2R X 4 DDR2 RDIMM APPLICATIONS	2023	JEDEC	
39	JESD82-20A.01	FBDIMM: ADVANCED MEMORY BUFFER (AMB)	2023	JEDEC	
40	JESD82-22.01	INSTRUMENTATION CHIP DATA SHEET FOR FBDIMM DIAGNOSTIC SENSELINES	2023	JEDEC	
41	JESD82-23.01	DEFINITION OF the SSTUA32S869 AND SSTUA32D869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS	2023	JEDEC	
42	JESD82-24.01	DEFINITION OF the SSTUB32865 28-bit 1:2 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS	2023	JEDEC	
43	JESD82-25.01	DEFINITION OF the SSTUB32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS	2023	JEDEC	
44	JESD82-26.01	DEFINITION OF THE SSTUB32868 REGISTERED BUFFER WITH PARITY FOR 2R x 4 DDR2 RDIMM APPLICATIONS	2023	JEDEC	
45	JESD82-27.01	Definition of the SSTUB32869 Registered Buffer with Parity for DDR2 RDIMM Applications	2023	JEDEC	
46	JESD82-31A.01	DDR4 REGISTERING CLOCK DRIVER (DDR4RCD02)	2023	JEDEC	
47	JESD82-3B.01	DEFINITION OF THE SSTV16857 2.5 V, 14-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS:	2023	JEDEC	
48	JESD82-512	DDR5 Registering Clock Driver Definition (DDR5RCD02)	2023	JEDEC	
49	JESD82-531	DDR5 Clock Driver Definition (DDR5CK01)	2023	JEDEC	
50	JESD82-6A.01	DEFINITION OF THE SSTV32852 2.5 V 24-BIT TO 48-BIT SSTL_2 REGISTERED BUFFER FOR 1U STACKED DDR DIMM APPLICATIONS:	2023	JEDEC	
51	JESD82-7A.01	DEFINITION OF THE SSTU32864 1.8 V CONFIGURABLE REGISTERED BUFFER FOR DDR2 RDIMM APPLICATIONS:	2023	JEDEC	
52	JESD93A	HYBRIDS/MCM	2023	JEDEC	
53	JESD96A.01	RADIO FRONT END - BASEBAND (RF-BB) INTERFACE	2023	JEDEC	
54	JESD87	STANDARD TEST STRUCTURE FOR RELIABILITY ASSESSMENT OF AlCu METALLIZATIONS WITH BARRIER MATERIALS	2023	JEDEC	
55	JM5.01	JEDEC Legal Guidelines	2023	JEDEC	
56	JS-001-2023	JOINT JEDEC/ESDA STANDARD FOR ELECTROSTATIC DISCHARGE SENSITIVITY TEST - HUMAN BODY MODEL (HBM) - COMPONENT LEVEL	2023	JEDEC	
57	JS-002-2022	ESDA/JEDEC JOINT STANDARD FOR ELECTROSTATIC DISCHARGE SENSITIVITY TESTING _ CHARGED DEVICE MODEL (CDM) DEVICE LEVEL	2023	JEDEC	
58	JESD91B	METHOD FOR DEVELOPING ACCELERATION MODELS FOR ELECTRONIC DEVICE FAILURE MECHANISMS	2022	JEDEC	
59	JM21U	JEDEC Manual of Organization and Procedure	2022	JEDEC	
60	JM12B	JEDEC COMMITTEE SPECIFIC ADDITIONAL POLICIES	2022	JEDEC	
61	JM18T	JEDEC COMMITTEE SCOPE MANUAL	2022	JEDEC	
62	JESD78F.01	IC LATCH-UP TEST	2022	JEDEC	
63	JESD8-20A.01	POD15 - 1.5 V PSEUDO OPEN DRAIN I/O	2022	JEDEC	
64	JESD8-21C.01	POD135 - 1.35 V PSEUDO OPEN DRAIN I/O	2022	JEDEC	
65	JESD8-30A.01	POD125 - 1.25 V PSEUDO OPEN DRAIN I/O	2022	JEDEC	
66	JESD625C	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES	2022	JEDEC	

67	JESD51-50A	OVERVIEW OF METHODOLOGIES FOR THE THERMAL MEASUREMENT OF SINGLE- AND MULTI-CHIP, SINGLE- AND MULTI-PN-JUNCTION LIGHT-EMITTING DIODES (LEDS)	2022	JEDEC	
68	JESD51-51A	IMPLEMENTATION OF THE ELECTRICAL TEST METHOD FOR THE MEASUREMENT OF REAL THERMAL RESISTANCE AND IMPEDANCE OF LIGHT-EMITTING DIODES WITH EXPOSED COOLING SURFACE	2022	JEDEC	
69	JESD51-52A	GUIDELINES FOR COMBINING CIE 127-2007 TOTAL FLUX MEASUREMENTS WITH THERMAL MEASUREMENTS OF LEDS WITH EXPOSED COOLING SURFACE	2022	JEDEC	
70	JESD51-53A	TERMS, DEFINITIONS AND UNITS GLOSSARY FOR LED THERMAL TESTING	2022	JEDEC	
71	JESD402-1A	TEMPERATURE RANGE AND MEASUREMENTS FOR COMPONENTS AND MODULES	2022	JEDEC	
72	JESD403-1B	JEDEC MODULE SIDEBAND BUS (SidebandBus)	2022	JEDEC	
73	JESD312	Automotive Solid State Drive (SSD) Device Standard	2022	JEDEC	
74	JESD301-2	PMIC5100 POWER MANAGEMENT IC STANDARD, Rev 1.03	2022	JEDEC	
75	JESD254	Secure Serial Flash Bus Transactions	2022	JEDEC	
76	JESD261	Serial NOR Security Hardware Abstraction Layer	2022	JEDEC	
77	JESD262	Customer Notification for Environmental Compliance Declaration Deviations	2022	JEDEC	
78	JESD251C	EXPANDED SERIAL PERIPHERAL INTERFACE (xSPI) FOR NONVOLATILE MEMORY DEVICES	2022	JEDEC	
79	JESD245E	BYTE ADDRESSABLE ENERGY BACKED INTERFACE	2022	JEDEC	
80	JESD305-R4-RCB	DDR5 RDIMM Standard Annex B	2022	JEDEC	
81	JESD305-R4-RCF	DDR5 RDIMM Standard, Annex F	2022	JEDEC	
82	JESD305-R8-RCA	DDR5 RDIMM Standard Annex A	2022	JEDEC	
83	JESD305-R8-RCC	DDR5 RDIMM Standard, Annex C	2022	JEDEC	
84	JESD305-R8-RCD	DDR5 RDIMM Standard Annex D	2022	JEDEC	
85	JESD305-R8-RCE	DDR5 RDIMM Standard Annex E	2022	JEDEC	
86	JESD305	DDR5 Load Reduced (LRDIMM) and Registered Dual Inline Memory Module (RDIMM) Common Specification	2022	JEDEC	
87	JESD308-U0-RCA	DDR5 UDIMM Raw Card Annex A	2022	JEDEC	
88	JESD308-U0-RCB	DDR5 UDIMM Raw Card Annex B	2022	JEDEC	
89	JESD308-U0-RCC	DDR5 UDIMM Raw Card Annex C	2022	JEDEC	
90	JESD308-U4-RCD	DDR5 UDIMM Raw Card Annex D	2022	JEDEC	
91	JESD308-U4-RCE	DDR5 UDIMM Raw Card Annex E	2022	JEDEC	
92	JESD308	DDR5 Unbuffered Dual Inline Memory Module (UDIMM) Common Standard	2022	JEDEC	
93	JESD309-S0-RCA	DDR5 SODIMM Raw Card Annex A Version 1	2022	JEDEC	
94	JESD309-S0-RCB	DDR5 SODIMM Raw Card Annex B. Version 1.0	2022	JEDEC	
95	JESD309-S0-RCC	DDR5 SODIMM Raw Card Annex C Version 1	2022	JEDEC	

96	JESD309-S4-RCD	DDR5 SODIMM Raw Card Annex D Version 1.0	2022	JEDEC	
97	JESD309-S4-RCE	DDR5 SODIMM Raw Card Annex E	2022	JEDEC	
98	JESD309	DDR5 Small Outline Dual Inline Memory Module (SODIMM) Common Standard	2022	JEDEC	
99	JESD231	Universal Flash Storage (UFS) File Based Optimizations (FBO) Extension, Version 1.0	2022	JEDEC	
100	JESD22-B120	Wire Bond Pull Test Methods	2022	JEDEC	
101	JESD22-B130	TEST METHOD FOR ESTABLISHING X-RAY TOTAL DOSE LIMIT FOR DRAM DEVICES	2022	JEDEC	
102	JESD22-A120C	TEST METHOD FOR THE MEASUREMENT OF MOISTURE DIFFUSIVITY AND WATER SOLUBILITY IN ORGANIC MATERIALS USED IN ELECTRONIC DEVICES	2022	JEDEC	
103	JESD22-B101D	EXTERNAL VISUAL	2022	JEDEC	
104	JEP190	Guideline for Evaluating dv/dt Robustness of SiC Power Devices, Version 1.0	2022	JEDEC	
105	JESD22-A108G	TEMPERATURE, BIAS, AND OPERATING LIFE	2022	JEDEC	
106	JESD216F.02	SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP)	2022	JEDEC	
107	JESD217A.01	TEST METHODS TO CHARACTERIZE VOIDING IN PRE-SMT BALL GRID ARRAY PACKAGES	2022	JEDEC	
108	JESD219A.01	SOLID-STATE DRIVE (SSD) ENDURANCE WORKLOADS	2022	JEDEC	
109	JEP132A.01	PROCESS CHARACTERIZATION GUIDELINE	2022	JEDEC	
110	JEP164	SYSTEM LEVEL ESD Part III: Review of ESD Testing and Impact on System-Efficient ESD Design (SEED)	2022	JEDEC	
111	JEP157A	RECOMMENDED ESD-CDM TARGET LEVELS	2022	JEDEC	
112	JEP160A	LONG-TERM STORAGE GUIDELINES FOR ELECTRONIC SOLID-STATE WAFERS, DICE, AND DEVICES	2022	JEDEC	
113	JEP151A	Test Procedure for the Measurement of Terrestrial Cosmic Ray Induced Destructive Effects in Power Semiconductor Devices	2022	JEDEC	
114	J-STD-035A	JOINT IPC/JEDEC Standard for Acoustic Microscopy for Non-Hermetic Encapsulated Electronic Devices	2022	JEDEC	
115	J-STD-020F	JOINT IPC/JEDEC Standard Moisture/Reflow Sensitivity Classification for Non-hermetic Surface Mount Devices (SMDs)	2022	JEDEC	
116	JEP149.01	APPLICATION THERMAL DERATING METHODOLOGIES:	2021	JEDEC	
117	JEP162A.01	SYSTEM LEVEL ESD: PART II: IMPLEMENTATION OF EFFECTIVE ESD ROBUST DESIGNS	2021	JEDEC	
118	JEP182	TEST METHOD FOR CONTINUOUS-SWITCHING EVALUATION OF GALLIUM NITRIDE POWER CONVERSION DEVICES	2021	JEDEC	
119	JEP178	ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING _ REPORTING ESD WITHSTAND LEVELS ON DATASHEETS	2021	JEDEC	
120	JEP180.01	GUIDELINE FOR SWITCHING RELIABILITY EVALUATION PROCEDURES FOR GALLIUM NITRIDE POWER CONVERSION DEVICES	2021	JEDEC	
121	JEP184	GUIDELINE FOR EVALUATING BIAS TEMPERATURE INSTABILITY OF SILICON CARBIDE METAL-OXIDE-SEMICONDUCTOR DEVICES FOR POWER ELECTRONIC CONVERSION	2021	JEDEC	
122	JEP185	COPY-EXACT PROCESS FOR MANUFACTURING	2021	JEDEC	
123	JEP186	Guideline to Specify a Transient Off-State Withstand Voltage Robustness Indicator in Datasheets for Lateral GaN Power Conversion Devices, Version 1.0	2021	JEDEC	
124	JEP187	Guidelines for Representing Switching Losses of SIC MOSFETs in Datasheets	2021	JEDEC	
125	JEP300-1	NEAR-TERM DRAM LEVEL ROWHAMMER MITIGATION	2021	JEDEC	
126	JEP301-1	SYSTEM LEVEL ROWHAMMER MITIGATION	2021	JEDEC	
127	JESD22-A110E.01	HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)	2021	JEDEC	
128	JESD22-A101D.01	STEADY-STATE TEMPERATURE-HUMIDITY BIAS LIFE TEST	2021	JEDEC	

129	JESD22-A118B.01	ACCELERATED MOISTURE RESISTANCE - UNBIASED HAST	2021	JEDEC	
130	JESD22-B109C	FLIP CHIP TENSILE PULL	2021	JEDEC	
131	JESD22-B118A	SEMICONDUCTOR WAFER AND DIE BACKSIDE EXTERNAL VISUAL INSPECTION	2021	JEDEC	
132	JESD233	XFM DEVICE, Version 1.0	2021	JEDEC	
133	JESD243A	COUNTERFEIT ELECTRONIC PARTS: NON-PROLIFERATION FOR MANUFACTURERS	2021	JEDEC	
134	JESD252.01	SERIAL FLASH RESET SIGNALING PROTOCOL	2021	JEDEC	
135	JESD253.01	ENCLOSURE FORM FACTOR FOR SSD DEVICES, VERSION 1.0	2021	JEDEC	
136	JESD251-1.01	Addendum No. 1 to JESD251 - OPTIONAL x4 QUAD I/O WITH DATA STROBE	2021	JEDEC	
137	JESD260	REPLAY PROTECTED MONOTONIC COUNTER (RPMC) FOR SERIAL FLASH DEVICES	2021	JEDEC	
138	JESD304-4.01	DDR4 NVDIMM-P BUS PROTOCOL	2021	JEDEC	
139	JESD315	Backup Energy Module Standard for NVDIMM Memory Devices (BEM)	2021	JEDEC	
140	JESD31F	GENERAL REQUIREMENTS FOR DISTRIBUTORS OF COMMERCIAL AND MILITARY SEMICONDUCTOR DEVICES	2021	JEDEC	
141	JESD79-4-1B	Addendum No. 1 to JESD79-4, 3D STACKED DRAM	2021	JEDEC	
142	JESD82-521	DDR5 Buffer Definition (DDR5DB01) - Rev. 1.1	2021	JEDEC	
143	JESD82-511	DDR5 REGISTERING CLOCK DRIVER DEFINITION (DDR5RCD01)	2021	JEDEC	
144	JESD85A	METHODS FOR CALCULATING FAILURE RATES IN UNITS OF FITS	2021	JEDEC	
145	JESD89-1B	TEST METHOD FOR REAL-TIME SOFT ERROR RATE	2021	JEDEC	
146	JESD89-2B	TEST METHOD FOR ALPHA SOURCE ACCELERATED SOFT ERROR RATE	2021	JEDEC	
147	JESD89-3B	TEST METHOD FOR BEAM ACCELERATED SOFT ERROR RATE	2021	JEDEC	
148	JESD89B	MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES	2021	JEDEC	
149	JESD8-34	1.05 V CMOS	2020	JEDEC	
150	JESD404-1	DDRx SPREAD SPECTRUM CLOCKING (SSC) STANDARD	2020	JEDEC	
151	JESD49B	PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD)	2020	JEDEC	
152	JESD246A	CUSTOMER NOTIFICATION PROCESS FOR DISASTERS	2020	JEDEC	
153	JESD220C-2.2	UNIVERSAL FLASH STORAGE, UFS 2.2	2020	JEDEC	
154	JESD22-B114B	MARK LEGIBILITY	2020	JEDEC	
155	JESD22-A105D	POWER AND TEMPERATURE CYCLING	2020	JEDEC	
156	JESD22-A113I	PRECONDITIONING OF NONHERMETIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING	2020	JEDEC	
157	JESD22-A100E	CYCLED TEMPERATURE HUMIDITY-BIAS WITH SURFACE CONDENSATION LIFE TEST	2020	JEDEC	
158	JEP181	ECXML Guidelines for Electronic Thermal System Level Models _ XML Requirements	2020	JEDEC	
159	JEP167A	CHARACTERIZATION OF INTERFACIAL ADHESION IN SEMICONDUCTOR PACKAGES	2020	JEDEC	
160	JEP121B	REQUIREMENTS FOR MICROELECTRONIC SCREENING AND TEST OPTIMIZATION:	2020	JEDEC	
161	JEP173	DYNAMIC ON-RESISTANCE TEST METHOD GUIDELINES FOR GaN HEMT BASED POWER CONVERSION DEVICES, VERSION 1.0	2019	JEDEC	
162	JEP143D	SOLID STATE RELIABILITY ASSESSMENT QUALIFICATION METHODOLOGIES	2019	JEDEC	
163	JESD22-B110B.01	MECHANICAL SHOCK _ DEVICE AND SUBASSEMBLY	2019	JEDEC	
164	JESD51-4A	THERMAL TEST CHIP GUIDELINE (WIRE BOND AND FLIP CHIP)	2019	JEDEC	
165	JESD82-32A	DDR4 DATA BUFFER DEFINITION (DDR4DB02)	2019	JEDEC	
166	JESD8-33	0.5 V LOW VOLTAGE SWING TERMINATED LOGIC (LVSTL05)	2019	JEDEC	

167	JESD88F	DICTIONARY OF TERMS FOR SOLID-STATE TECHNOLOGY, 7th Edition	2018	JEDEC	
168	JS709C	JOINT JEDEC/ECA STANDARD, DEFINITION OF _LOW-HALOGEN_ FOR ELECTRONIC PRODUCTS	2018	JEDEC	
169	JESD72A	TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS:	2018	JEDEC	
170	JESD50C	SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION AND OUTLIER MANAGEMENT	2018	JEDEC	
171	JESD8-31	1.8 V HIGH-SPEED LVCMOS (HS_LVCMOS) INTERFACE	2018	JEDEC	
172	JESD671D	DEVICE QUALITY PROBLEM ANALYSIS AND CORRECTIVE ACTION RESOLUTION METHODOLOGY	2018	JEDEC	
173	JESD22-B112B	PACKAGE WARPAGE MEASUREMENT OF SURFACE-MOUNT INTEGRATED CIRCUITS AT ELEVATED TEMPERATURE	2018	JEDEC	
174	JESD22-B113B	BOARD LEVEL CYCLIC BEND TEST METHOD FOR INTERCONNECT RELIABILITY CHARACTERIZATION OF SMT ICs FOR HANDHELD ELECTRONIC PRODUCTS	2018	JEDEC	
175	JESD22-B119	MECHANICAL COMPRESSIVE STATIC STRESS TEST METHOD	2018	JEDEC	
176	JESD22-A117E	ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST	2018	JEDEC	
177	JESD22-A111B	EVALUATION PROCEDURE FOR DETERMINING CAPABILITY TO BOTTOM SIDE BOARD ATTACH BY FULL BODY SOLDER IMMERSION OF SMALL SURFACE MOUNT SOLID STATE DEVICES	2018	JEDEC	
178	JEP131C	POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)	2018	JEDEC	
179	JEP155B	RECOMMENDED ESD TARGET LEVELS FOR HBM/MM QUALIFICATION	2018	JEDEC	
180	JEP156A	CHIP-PACKAGE INTERACTION UNDERSTANDING, IDENTIFICATION AND EVALUATION	2018	JEDEC	
181	JEP176	ADAPTER TEST BOARD RELIABILITY TEST GUIDELINES	2018	JEDEC	
182	JEP118A	GUIDELINES FOR GaAs MMIC PHEMT/MESFET AND HBT RELIABILITY ACCELERATED LIFE TESTING	2018	JEDEC	
183	JEP001-1A	FOUNDRY PROCESS QUALIFICATION GUIDELINES - BACKEND OF LIFE (Wafer Fabrication Manufacturing Sites)	2018	JEDEC	
184	JEP001-2A	FOUNDRY PROCESS QUALIFICATION GUIDELINES - FRONT END TRANSISTOR LEVEL (Wafer Fabrication Manufacturing Sites)	2018	JEDEC	
185	JEP001-3A	FOUNDRY PROCESS QUALIFICATION GUIDELINES PRODUCT LEVEL (Wafer Fabrication Manufacturing Sites)	2018	JEDEC	
186	J-STD-033D	JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING, AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES	2018	JEDEC	
187	TO-252F	Registration - Flange Mounted Family, Surface Mount, Peripheral Terminals. R-PSFM-G.	2017	JEDEC	0
188	JESD214.01	CONSTANT-TEMPERATURE AGING METHOD TO CHARACTERIZE COPPER INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING	2017	JEDEC	
189	JESD16B	ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM)	2017	JEDEC	
190	JESD22-B105E	LEAD INTEGRITY	2017	JEDEC	
191	JESD69C	INFORMATION REQUIREMENTS FOR THE QUALIFICATION OF SILICON DEVICES	2017	JEDEC	
192	JESD37A	STANDARD LOGNORMAL ANALYSIS OF UNCENSORED DATA, AND OF SINGLY RIGHT -CENSORED DATA UTILIZING THE PERSSON AND ROOTZEN METHOD:	2017	JEDEC	
193	JM19A	FILE NAMING CONVENTION:	2017	JEDEC	
194	AnnexA - JESD21C	Annex A: Differences between JESD21C Release 26 and its predecessor JESD21C, Release 26.	2017	JEDEC	0
195	JESD22-A108F	TEMPERATURE, BIAS, AND OPERATING LIFE	2017	JEDEC	0
196	JESD22-B116B	WIRE BOND SHEAR TEST	2017	JEDEC	0
197	MODULE4.20.25.A	Annex A, R/C A, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM SODIMM Design Specification	2017	JEDEC	0
198	MODULE4.20.25.C	Annex C, R/C C, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM SODIMM Design Specification	2017	JEDEC	0

199	MODULE4.20.25.E	Annex E, R/C E, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM SODIMM Design Specification	2017	JEDEC	0
200	MODULE4.20.26.B	Annex B, R/C B, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Unbuffered DIMM Design Specification	2017	JEDEC	0
201	MODULE4.20.28.B	Annex B, R/C B, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	2017	JEDEC	0
202	MODULE4.20.28.C	Annex C, R/C C, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	2017	JEDEC	0
203	DR-4.27E	Design Requirements - Ball Grid Array Package (BGA). (Covers body sizes >21mm)	2017	JEDEC	0
204	DR-4.5M	Design Requirements - Ball Grid Array Package (BGA) and Interstitial Ball Grid Array Package (IBGA). (Covers Body sizes ? 21 mm)	2017	JEDEC	0
205	GS-010B	Standard - DDR4 DIMM Socket Insertion and Extraction Force Gauge	2017	JEDEC	0
206	JEP106AV	STANDARD MANUFACTURERS IDENTIFICATION CODE	2017	JEDEC	0
207	JEP175	DDR4 PROTOCOL CHECKS	2017	JEDEC	0
208	JESD209-4-1	ADDENDUM NO. 1 to JESD209-4, LOW POWER DOUBLE DATA RATE 4X (LPDDR4X)	2017	JEDEC	0
209	JESD209-4B	LOW POWER DOUBLE DATA RATE 4 (LPDDR4)	2017	JEDEC	0
210	JESD210A	AVALANCHE BREAKDOWN DIODE (ABD) TRANSIENT VOLTAGE SUPPRESSORS	2017	JEDEC	0
211	JESD213A	STANDARD TEST METHOD UTILIZING X-RAY FLUORESCENCE (XRF) FOR ANALYZING COMPONENT FINISHES AND SOLDER ALLOYS TO DETERMINE TIN (Sn) - LEAD (Pb) CONTENT	2017	JEDEC	0
212	JESD224A	UNIVERSAL FLASH STORAGE (UFS) TEST	2017	JEDEC	0
213	JESD245B.01	BYTE ADDRESSABLE ENERGY BACKED INTERFACE	2017	JEDEC	0
214	JESD250	GRAPHICS DOUBLE DATA RATE 6 (GDDR6) SGRAM STANDARD	2017	JEDEC	0
215	JESD30H	DESCRIPTIVE DESIGNATION SYSTEM FOR ELECTRONIC-DEVICE PACKAGES	2017	JEDEC	0
216	JESD47J.01	STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS	2017	JEDEC	0
217	JESD659C	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING	2017	JEDEC	0
218	JESD79-4-1	Addendum No. 1 to JESD79-4, 3D Stacked DRAM	2017	JEDEC	0
219	JESD79-4B	DDR4 SDRAM STANDARD	2017	JEDEC	0
220	JESD9C	INSPECTION CRITERIA FOR MICROELECTRONIC PACKAGES AND COVERS	2017	JEDEC	0
221	JS-001-2017	JOINT JEDEC/ESDA STANDARD FOR ELECTROSTATIC DISCHARGE SENSITIVITY TEST - HUMAN BODY MODEL (HBM) - COMPONENT LEVEL	2017	JEDEC	0
222	MO-234C	Registration - Ball Grid Array Family, Rectangular, 1.00 mm Pitch. PBGA.	2017	JEDEC	0
223	MO-276L	Registration - Fine Pitch Ball Grid Array Family, Rectangular , 0.50 mm Pitch. FR-XBGA, (L,T,V)FR-XBGA.	2017	JEDEC	0
224	MO-317B.01	Registration - Upper PoP Ball Grid Array Family, Square, 0.40 mm Pitch. PBGA	2017	JEDEC	0
225	MO-318B	Registration - Ball Grid Array Family, Square, 1.00 mm Pitch. PBGA	2017	JEDEC	0
226	MO-321A.01	Registration - Upper PoP Ball Grid Array Family, Square, 0.50 mm Pitch. PBGA	2017	JEDEC	0
227	MO-322A.01	Registration - Upper PoP Ball Grid Array Family, Square, 0.65 mm Pitch. PBGA	2017	JEDEC	0
228	MO-323A.01	Registration - Upper PoP Ball Grid Array Family, Square, 0.40 mm Pitch. PBGA	2017	JEDEC	0
229	MO-328A	Registration - Ball Grid Array Family, Rectangle, 0.75 mm Pitch	2017	JEDEC	0
230	MO-329A	288 PIN DDR5 DIMM, 0.85 MM PITCH.	2017	JEDEC	0
231	MS-034G	Standard - Ball Grid Array Family, Square, 1.27 mm, and 1.50 mm Pitch. S-PBGA/PBGA.	2017	JEDEC	0
232	JM18R	JEDEC COMMITTEE SCOPE MANUAL	2017	JEDEC	0
233	SO-023A	DDR5 DIMM SMT 288 PIN SOCKET OUTLINE 0.85 MM PITCH. SKT	2017	JEDEC	0
234	SO-022A	Registration - 12 Pin UFS Socket Outline, 0.91 mm Pitch. SKT	2016	JEDEC	0

235	SO-016C.01	Registration - DDR4 DIMM PTH 288 Pin Socket Outline, 0.85 mm Pitch. SKT	2016	JEDEC	0
236	SO-017C.01	Registration - DDR4 DIMM SMT, 288 Pin Socket Outline, 0.85 mm Pitch. SKT	2016	JEDEC	0
237	SO-019C.01	REGISTRATION - DDR4 DIMM Press Fit 288 Pin Socket Outline, 0.85 mm Pitch. SKT	2016	JEDEC	0
238	PS-003A.01	DDR4 260 Pin SODIMM Connector Performance Standard	2016	JEDEC	0
239	MO-324A	Registration - Lower PoP Ball Grid Array Family, Square, 0.50 mm Top, 0.50 mm Bottom Pitch. S-XBGA	2016	JEDEC	0
240	MO-325A	Registration - Lower PoP Ball Grid Array Family, Square, 0.65 mm Top, 0.50 mm Bottom Pitch. S-XBGA	2016	JEDEC	0
241	MO-326A	Registration - Lower PoP Ball Grid Array Family, Square, 0.80 mm Top, 0.50 mm Bottom Pitch. S-XBGA	2016	JEDEC	0
242	MO-327A	Registration - 9 Lead Surface Mount Power Package, 1.2 mm Pitch. H-PSOF	2016	JEDEC	0
243	MO-319A	Registration - 6 Lead Surface Mount Power Package with Fused Leads. H-PSOF	2016	JEDEC	0
244	MO-320A	Registration - 12 Pin UFS Card, 0.91 mm Pitch	2016	JEDEC	0
245	MO-314A.02	Registration - 288 PIN DDR4 MINI DIMM, 0.50 MM PITCH	2016	JEDEC	0
246	MO-302C	Registration - Lower PoP Ball Grid Array Family, SQUARE, 0.40 mm Top, 0.40 mm Bottom Pitch. S-XBGA.	2016	JEDEC	0
247	JM12A	JEDEC COMMITTEE SPECIFIC ADDITIONAL POLICIES	2016	JEDEC	0
248	MO-210N	Registration - Fine Pitch Ball Grid Array Family, Rectangular, 0.80 mm Pitch. (V,T,L)FR-XBGA.	2016	JEDEC	0
249	JESD8-29	0.6 V LOW VOLTAGE SWING TERMINATED LOGIC (LVSTL06)	2016	JEDEC	0
250	JESD82-31	DDR4 REGISTERING CLOCK DRIVER (DDR4RCD01)	2016	JEDEC	0
251	JESD82-32	DDR4 DATA BUFFER DEFINITION (DDR4DB01)	2016	JEDEC	0
252	JESD78E	IC LATCH-UP TEST	2016	JEDEC	0
253	JESD243	COUNTERFEIT ELECTRONIC PARTS: NON-PROLIFERATION FOR MANUFACTURERS	2016	JEDEC	0
254	JESD31E	GENERAL REQUIREMENTS FOR DISTRIBUTORS OF COMMERCIAL AND MILITARY SEMICONDUCTOR DEVICES	2016	JEDEC	0
255	JESD247	MULTI-WIRE MULTI-LEVEL I/O STANDARD	2016	JEDEC	0
256	JESD248	DDR4 NVDIMM-N DESIGN STANDARD (Revision 1.0)	2016	JEDEC	0
257	JESD212C	GRAPHICS DOUBLE DATA RATE (GDDR5) SGRAM STANDARD	2016	JEDEC	0
258	JESD225	UNIVERSAL FLASH STORAGE (UFS) SECURITY EXTENSION	2016	JEDEC	0
259	JESD230C	NAND FLASH INTERFACE INTEROPERABILITY	2016	JEDEC	0
260	JESD232A	GRAPHICS DOUBLE DATA RATE (GDDR5X) SGRAM STANDARD	2016	JEDEC	0
261	JESD223-1A	UNIVERSAL FLASH STORAGE HOST CONTROLLER INTERFACE (UFSHCI), UNIFIED MEMORY EXTENSION, Version 1.1A	2016	JEDEC	0
262	JESD223C	UNIVERSAL FLASH STORAGE HOST CONTROLLER INTERFACE (UFSHCI), Version 2.1	2016	JEDEC	0
263	JESD227	EMBEDDED MULTIMEDIACARD (e MMC) SECURITY EXTENSION	2016	JEDEC	0
264	JESD217.01	TEST METHODS TO CHARACTERIZE VOIDING IN PRE-SMT BALL GRID ARRAY PACKAGES	2016	JEDEC	0
265	JESD218B.01	SOLID STATE DRIVE (SSD) REQUIREMENTS AND ENDURANCE TEST METHOD	2016	JEDEC	0
266	JESD220-1A	UNIVERSAL FLASH STORAGE (UFS) UNIFIED MEMORY EXTENSION, Version 1.1	2016	JEDEC	0
267	JESD220-2	UNIVERSAL FLASH STORAGE (UFS) CARD EXTENSION, Version 1.0	2016	JEDEC	0
268	JESD220C	UNIVERSAL FLASH STORAGE (UFS), Version 2.1	2016	JEDEC	0
269	JEP174	UNDERSTANDING ELECTRICAL OVERSTRESS - EOS	2016	JEDEC	0
270	J-STD-609B	MARKING, SYMBOLS, AND LABELS OF LEADED AND LEAD-FREE TERMINAL FINISHED MATERIALS USED IN ELECTRONIC ASSEMBLY	2016	JEDEC	0
271	JEP122H	FAILURE MECHANISMS AND MODELS FOR SEMICONDUCTOR DEVICES	2016	JEDEC	0
272	J-STD-046	CUSTOMER NOTIFICATION STANDARD FOR PRODUCT/PROCESS CHANGES BY ELECTRONIC PRODUCT SUPPLIERS	2016	JEDEC	0

273	JEP130B	GUIDELINES FOR PACKING AND LABELING OF INTEGRATED CIRCUITS IN UNIT CONTAINER PACKING (Tubes, Trays, and Tape and Reel)	2016	JEDEC	0
274	JEP166B	JC-42.6 MANUFACTURER IDENTIFICATION (ID) CODE FOR LOW POWER MEMORIES	2016	JEDEC	0
275	DG-4.20F	Design Requirements - Small Scale Plastic Quad and Dual Inline, Square and Rectangular, No-Lead Packages (With Optional Thermal Enhancements). Small Scale (QFN/SON).	2016	JEDEC	0
276	DG-4.24B	Design Requirements - Scalable Quad Flat No-lead Packages, Square and Rectangular (Scalable QFN)	2016	JEDEC	0
277	DG-4.25B	Design Requirements - Fine-Pitch, Land Grid Array Package, Square and Rectangular (FLGA, FRLGA)	2016	JEDEC	0
278	MODULE4.20. 28.H	Annex H, Raw Card H, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	2016	JEDEC	0
279	MODULE4.20. 28.J	Annex J, Raw Card J, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	2016	JEDEC	0
280	MODULE4.20. 28.D	Annex D, Raw Card D, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	2016	JEDEC	0
281	MODULE4.20. 28.E	Annex E, R/C E, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	2016	JEDEC	0
282	MODULE4.20. 27.D	Annex D, R/C D, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification	2016	JEDEC	0
283	MODULE4.20. 25	260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM SODIMM Design Specification	2016	JEDEC	0
284	MODULE4.20. 28.A	Annex A, R/C A, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	2016	JEDEC	0
285	MODULE4.20. 26.C	Annex C, Raw Card C, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Unbuffered DIMM Design Specification	2016	JEDEC	0
286	MODULE4.20. 25.G	Annex G, Raw Card G, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM SODIMM Design Specification	2016	JEDEC	0
287	MODULE4.20. 25.H	Annex H, Raw Card H, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM SODIMM Design Specification	2016	JEDEC	0
288	MODULE4.20. 26	288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Unbuffered DIMM Design Specification	2016	JEDEC	0
289	MODULE4.20. 25.B	Annex B, Raw Card B, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM SO-DIMM Design Specification	2016	JEDEC	0
290	JESD22-B111A	BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS	2016	JEDEC	0
291	JESD22-A122A	POWER CYCLING	2016	JEDEC	0
292	JESD22-B103B.01	VIBRATION, VARIABLE FREQUENCY	2016	JEDEC	0
293	JESD22-B106E	RESISTANCE TO SOLDER SHOCK FOR THROUGH-HOLE MOUNTED DEVICES	2016	JEDEC	0
294	JESD22-A106B.01	THERMAL SHOCK	2016	JEDEC	0
295	JESD22-A113H	PRECONDITIONING OF NONHERMETIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING	2016	JEDEC	0
296	JESD22-B115A.01	SOLDER BALL PULL	2016	JEDEC	0
297	MCP3.12.1	Multichip Packages (MCP) and Discrete eMMC, e2MMC, and UFS	2016	JEDEC	0
298	SPD4.1.2.L-4	SPD Annex L, Serial Presence Detect (SPD) for DDR4 SDRAM Modules, Release 4	2016	JEDEC	0
299	SPD4.1.2.M-2	Annex M, Serial Presence Detect (SPD) for LPDDR3 and LPDDR4 SDRAM Modules, Document Release 2	2016	JEDEC	0
300	SPD4.1.6	EE1004 and TSE2004 Device Specification - Definitions of the EE1004-v 4 Kbit Serial Presence Detect (SPD) EEPROM and TSE2004av 4 Kbit SPD EEPROM with Temperature Sensor (TS) for Memory Module Applications	2016	JEDEC	0

301	SPP-025B	Standard Practices and Procedures - Package Variation Designators	2016	JEDEC	0
302	SPD4.1.2.M-1	Annex M: Serial Presence Detect (SPD) for LPDDR3 and LPDDR4 SDRAM Modules, Release 1	2015	JEDEC	0
303	SPD4.1.2.L-3	SPD Annex L: Serial Presence Detect (SPD) for DDR4 SDRAM Modules, Release 3	2015	JEDEC	0
304	JESD22-A119A	LOW TEMPERATURE STORAGE LIFE	2015	JEDEC	0
305	JESD22-A101D	STEADY-STATE TEMPERATURE-HUMIDITY BIAS LIFE TEST	2015	JEDEC	0
306	JESD22-A102E	ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE	2015	JEDEC	0
307	JESD22-A110E	HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)	2015	JEDEC	0
308	JESD22-A118B	ACCELERATED MOISTURE RESISTANCE - UNBIASED HAST	2015	JEDEC	0
309	JESD22-A103E	HIGH TEMPERATURE STORAGE LIFE	2015	JEDEC	0
310	JESD22-B101C	EXTERNAL VISUAL	2015	JEDEC	0
311	MODULE4.20.26.A	Annex A, R/C A, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Unbuffered DIMM Design Specification	2015	JEDEC	0
312	MODULE4.20.26.D	Annex D, R/C D, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Unbuffered DIMM Design Specification	2015	JEDEC	0
313	MODULE4.20.26.E	Annex E, R/C E, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Unbuffered DIMM Design Specification	2015	JEDEC	0
314	MODULE4.20.27	288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification	2015	JEDEC	0
315	MODULE4.20.27.E	Annex E, R/C E, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification	2015	JEDEC	0
316	MODULE4.20.28	288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	2015	JEDEC	0
317	MODULE4.20.28.F	Annex F, R/C F, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	2015	JEDEC	0
318	MODULE4.20.28.G	Annex G, R/C G, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Registered DIMM Design Specification	2015	JEDEC	0
319	DG-4.14H	Design Requirements - Ball Grid Array Package (BGA)	2015	JEDEC	0
320	DO-219C	Registration - Plastic, Small Outline, Flat Lead, surface mount package. R-PDSO-F2. Item 10-455.	2015	JEDEC	0
321	DR-4.26B	Design Requirements - Micropillar Grid Array (MPGA)	2015	JEDEC	0
322	JEP159A	PROCEDURE FOR THE EVALUATION OF LOW-k/METAL INTER/INTRA-LEVEL DIELECTRIC INTEGRITY	2015	JEDEC	0
323	JEP151	Test Procedure for the Measurement of Terrestrial Cosmic Ray Induced Destructive Effects in Power Semiconductor Devices	2015	JEDEC	0
324	JEP172A	DISCONTINUING USE OF THE MACHINE MODEL FOR DEVICE ESD QUALIFICATION	2015	JEDEC	0
325	JEP163	SELECTION OF BURN-IN/LIFE TEST CONDITIONS AND CRITICAL PARAMETERS FOR QML MICROCIRCUITS	2015	JEDEC	0
326	JESD8-28	300 mV INTERFACE	2015	JEDEC	0
327	JESD209-3C	LOW POWER DOUBLE DATA RATE 3 SDRAM (LPDDR3)	2015	JEDEC	0
328	JESD235A	HIGH BANDWIDTH MEMORY (HBM) DRAM	2015	JEDEC	0
329	JESD241	PROCEDURE FOR WAFER-LEVEL DC CHARACTERIZATION OF BIAS TEMPERATURE INSTABILITIES	2015	JEDEC	0
330	JESD557C	STATISTICAL PROCESS CONTROL SYSTEMS	2015	JEDEC	0
331	JESD84-B51	EMBEDDED MULTI-MEDIA CARD (e MMC), ELECTRICAL STANDARD (5.1)	2015	JEDEC	0
332	JM21R	JEDEC Manual of Organization and Procedure	2015	JEDEC	0
333	JESD94B	APPLICATION SPECIFIC QUALIFICATION USING KNOWLEDGE BASED TEST METHODOLOGY	2015	JEDEC	0

334	JS002-2014	ESDA/JEDEC JOINT STANDARD FOR ELECTROSTATIC DISCHARGE SENSITIVITY TESTING _ CHARGED DEVICE MODEL (CDM) DEVICE LEVEL	2015	JEDEC	0
335	JS709B	JOINT JEDEC/ECA STANDARD, DEFINITION OF LOW-HALOGEN FOR ELECTRONIC PRODUCTS	2015	JEDEC	0
336	MO-299B	Registration - Surface Mount Power Package with fused leads. H-PSOF	2015	JEDEC	0
337	MO-300C	Registration - mSATA SSD Assembly. DIM.	2015	JEDEC	0
338	MO-286B	Registration - Plastic Small Outline, Wide Body SOIC, 7.5 Body Width, 0.65 Pitch. R-PDSO.	2015	JEDEC	0
339	MO-246G	Registration - Rectangular, Fine Pitch, Thin Ball Grid Array, 0.65 mm pitch. TFR-XBGA.	2015	JEDEC	0
340	MO-315A	Registration - Dual Pitch Number Ball Grid Array Family, Square, 0.80 mm Major, 0.65 mm Minor Pitch. (T,V)F-SBGA	2015	JEDEC	0
341	MO-316A	Registration - HBM Micropillar Grid Array Package (MPGA)	2015	JEDEC	0
342	MO-309F	Registration - 288 Pin DDR4 DIMM, 0.85 mm Pitch. DIMM	2015	JEDEC	0
343	PS-002A	Performance Standard - DDR4 288 Pin U/R/LR DIMM Connector Performance Standard	2015	JEDEC	0
344	MS-013F	Standard - Very Thick Profile, Plastic Small Outline (SO) Family, 1.27 mm pitch, 7.50 mm (.300 inch) Body Width. B1R-PDSO/SOP/SOIC.	2015	JEDEC	0
345	SO-018D	Registration - DDR4 Small Outline Dual Inline Memory Module (SODIMM), 260 pin, 0.50 mm pitch Socket Outline	2015	JEDEC	0
346	SO-021A	Registration - DDR4 MiniDIMM SMT 288 pin socket outline 0.50 mm pitch	2015	JEDEC	0
347	SPP-010B	Standard Practices and Procedures - Grid Array Terminal Position Numbering	2014	JEDEC	0
348	SPP-013A	Standard Practices and Procedures - Registered and Standard Outlines	2014	JEDEC	0
349	SO-020A	Registration - DDR3 Single Sided SODIMM 204 Pin Socket Outline with 0.60 mm Pitch. SKT	2014	JEDEC	0
350	PRN14-NM10	PC4-RDIMM_090_Annex-F	2014	JEDEC	0
351	PRN14-NM1	DDR4 UDIMM Design Specification Annex D	2014	JEDEC	0
352	MO-310C	Registration - 260 Pin DDR4 SODIMM, 0.50 mm Pitch. DIMM	2014	JEDEC	0
353	MO-311D	Registration - Dual-Pitch, Thin and Very Thin Profile, Rectangular Die Size BGA, 0.80 mm X 0.65 mm Pitch. (T,V)FR-xDSBGA	2014	JEDEC	0
354	MO-313A	Registration - Fine Pitch Ball Grid Array Family, Square, 0.50 mm pitch. (T, V) F-SBGA	2014	JEDEC	0
355	MO-274D	Registration - DDR1/DDR2/DDR3, 144 Pin, 16b/32b Small Outline Dual Inline Memory Module (SODIMM) Family, 0.8 mm Pitch. DIMM	2014	JEDEC	0
356	MO-268E	Registration - 204 Pin DDR3 SODIMM w/ 0.60 mm Pitch. DIM	2014	JEDEC	0
357	MO-269J	Registration - 240 Pin DDR3 DIMM (Dual Inline Memory Module) Family with 1.00 mm pitch. DIM	2014	JEDEC	0
358	JESD82-30	LRDIMM DDR3 MEMORY BUFFER (MB)	2014	JEDEC	0
359	JP001A	FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites)	2014	JEDEC	0
360	JESD8-22B	HSUL 12 LPDDR2 AND LPDDR3 I/O WITH OPTIONAL ODT	2014	JEDEC	0
361	JESD84-B50.1	Embedded Multi-Media Card (e_MMC) Electrical Standard (5.01)	2014	JEDEC	0
362	JESD246	CUSTOMER NOTIFICATION PROCESS FOR DISASTERS	2014	JEDEC	0
363	JESD237	RELIABILITY QUALIFICATION OF POWER AMPLIFIER MODULES	2014	JEDEC	0
364	JESD229-2	WIDE I/O 2 (WideIO2)	2014	JEDEC	0
365	JESD216B	SERIAL FLASH DISCOVERABLE PARAMETERS (SFDP)	2014	JEDEC	0
366	JEP171	GDDR5 MEASUREMENT PROCEDURES	2014	JEDEC	0
367	JEP148B	RELIABILITY QUALIFICATION OF SEMICONDUCTOR DEVICES BASED ON PHYSICS OF FAILURE RISK AND OPPORTUNITY ASSESSMENT	2014	JEDEC	0
368	JEP153A	CHARACTERIZATION AND MONITORING OF THERMAL STRESS TEST OVEN TEMPERATURES	2014	JEDEC	0
369	J-STD-048	JOINT JEDEC/IPC/ECIA STANDARD - NOTIFICATION STANDARD FOR PRODUCT DISCONTINUANCE	2014	JEDEC	0
370	J-STD-020E	JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SURFACE-MOUNT DEVICES	2014	JEDEC	0

371	DO-218C	Registration - Power Outline, Plastic Surface Mount C-Bend	2014	JEDEC	0
372	DG-4.7F	Design Requirements - Die-Size Ball Grid Array Packages (DSBGA) Design Guide.	2014	JEDEC	0
373	MODULE4.20.TOC	Dual Inline Memory Modules (DIMMs) Table of Contents	2014	JEDEC	0
374	MODULE4.20.27.A	Annex A, Raw Card A, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification	2014	JEDEC	0
375	MODULE4.20.27.B	Annex B, Raw Card B, in 288-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM Load Reduced DIMM Design Specification	2014	JEDEC	0
376	MODULE4.20.25.F	Annex F, R/C F, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM SODIMM Design Specification	2014	JEDEC	0
377	MODULE4.20.25.D	Annex D, R/C D, in 260-Pin, 1.2 V (VDD), PC4-1600/PC4-1866/PC4-2133/PC4-2400/PC4-2666/PC4-3200 DDR4 SDRAM SO-DIMM Design Specification	2014	JEDEC	0
378	MODULE4.20.24	240-Pin, 72 bit-wide, PC3(L)-6400/PC3(L)-8500/PC3(L)-10600/PC3(L)-12800/PC3(L)-14900/PC3(L)-17000 DDR3 SDRAM Load Reduced DIMM Design Specification	2014	JEDEC	0
379	MODULE4.20.24.A	Annex A, R/C A, in 240-Pin, 72 bit-wide, PC3(L)-6400/PC3(L)-8500/PC3(L)-10600/PC3(L)-12800/PC3(L)-14900/PC3(L)-17000 DDR3 SDRAM Load Reduced DIMM Design Specification	2014	JEDEC	0
380	MODULE4.20.24.C	Annex C, R/C C, in 240-Pin, 72 bit-wide, PC3(L)-6400/PC3(L)-8500/PC3(L)-10600/PC3(L)-12800/PC3(L)-14900/PC3(L)-17000 DDR3 SDRAM Load Reduced DIMM Design Specification	2014	JEDEC	0
381	MODULE4.20.24.K	Annex K, R/C K, in 240-Pin, 72 bit-wide, PC3(L)-6400/PC3(L)-8500/PC3(L)-10600/PC3(L)-12800/PC3(L)-14900/PC3(L)-17000 DDR3 SDRAM Load Reduced DIMM Design Specification	2014	JEDEC	0
382	MODULE4.20.18	204-Pin DDR3 SDRAM Unbuffered SODIMM Design Specification	2014	JEDEC	0
383	JESD22-B109B	FLIP CHIP TENSILE PULL	2014	JEDEC	0
384	JESD22-B117B	SOLDER BALL SHEAR	2014	JEDEC	0
385	JESD22-A104E	TEMPERATURE CYCLING	2014	JEDEC	0
386	JESD22-A120B	TEST METHOD FOR THE MEASUREMENT OF MOISTURE DIFFUSIVITY AND WATER SOLUBILITY IN ORGANIC MATERIALS USED IN INTEGRATED CIRCUITS:	2014	JEDEC	0
387	SPD4.1.2.L-2	SPD Annex L: Serial Presence Detect (SPD) for DDR4 SDRAM Modules, Release 2	2014	JEDEC	0
388	SPD4.1.2.11	SPD Annex K - Serial Presence Detect (SPD) for DDR3 SDRAM Modules, Release 6	2014	JEDEC	0
389	SPD4.1.2.L-1	SPD Annex L: Serial Presence Detect (SPD) for DDR4 SDRAM Modules, Release 1	2013	JEDEC	0
390	JESD22-A107C	SALT ATMOSPHERE	2013	JEDEC	0
391	JESD22-C101F	FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS	2013	JEDEC	0
392	MODULE4.20.19	240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Unbuffered DIMM Design Specification	2013	JEDEC	0
393	MODULE4.20.21 Annex C	204-Pin EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM 72b-SO-DIMM Design Specification	2013	JEDEC	0
394	MODULE4.20.21.D	204-Pin EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM 72b-SODIMM Design Specification	2013	JEDEC	0
395	MODULE4.20.22.B	144-Pin EP3-3200/EP3-4200/EP3-5300/EP3-6400 Unbuffered 32b-SO-DIMM Design Specification	2013	JEDEC	0
396	MODULE4.20.22.D	144-Pin EP3-3200/EP3-4200/EP3-5300/EP3-6400 Unbuffered 32b-SO-DIMM Design Specification	2013	JEDEC	0
397	MODULE4.20.23.AD	R/C AD, in 240-Pin, 72 bit-wide, PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification	2013	JEDEC	0
398	MODULE4.20.23.M	R/C M, in 240-Pin, 72 bit-wide, PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification	2013	JEDEC	0

399	DO-201B	Registration - Lead Mounted Family, Axial Type, Chamfer (Round) Body Diode. PALF (Ref. DO-27, DO-32, DO-39)	2013	JEDEC	0
400	JEP167	CHARACTERIZATION OF INTERFACIAL ADHESION IN SEMICONDUCTOR PACKAGES	2013	JEDEC	0
401	JEP170	GUIDELINES FOR VISUAL INSPECTION AND CONTROL OF FLIP CHIP TYPE COMPONENTS (FCxGA)	2013	JEDEC	0
402	JEP150.01	STRESS-TEST-DRIVEN QUALIFICATION OF AND FAILURE MECHANISMS ASSOCIATED WITH ASSEMBLED SOLID STATE SURFACE-MOUNT COMPONENTS	2013	JEDEC	0
403	JEP162	SYSTEM LEVEL ESD: PART II: IMPLEMENTATION OF EFFECTIVE ESD ROBUST DESIGNS	2013	JEDEC	0
404	JEP70C	GUIDE TO STANDARDS AND PUBLICATIONS RELATING TO QUALITY AND RELIABILITY OF ELECTRONIC HARDWARE	2013	JEDEC	0
405	JESD209-2F	LOW POWER DOUBLE DATA RATE 2 (LPDDR2)	2013	JEDEC	0
406	JESD22-A100D	CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST	2013	JEDEC	0
407	JESD22-B110B	MECHANICAL SHOCK COMPONENT AND SUBASSEMBLY	2013	JEDEC	0
408	JESD234	TEST STANDARD FOR THE MEASUREMENT OF PROTON RADIATION SINGLE EVENT EFFECTS IN ELECTRONIC DEVICES	2013	JEDEC	0
409	JESD226	RF BIASED LIFE (RFBL) TEST	2013	JEDEC	0
410	JESD49A.01	PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD)	2013	JEDEC	0
411	JESD79-3-1A.01	Addendum No. 1 to JESD79-3 - 1.35 V DDR3L-800, DDR3L-1066, DDR3L-1333, DDR3L-1600, and DDR3L-1866	2013	JEDEC	0
412	JESD79-3-3	ADDENDUM No. 3 to JESD79-3 - 3D STACKED SDRAM	2013	JEDEC	0
413	JESD8-21A	POD135 - 1.35 V PSEUDO OPEN DRAIN I/O	2013	JEDEC	0
414	JESD88E	DICTIONARY OF TERMS FOR SOLID-STATE TECHNOLOGY, 6th Edition	2013	JEDEC	0
415	JMTest	JEDEC Test Document	2013	JEDEC	0
416	MO-193E	Registration - Plastic Thin Shrink Small Outline Package (Shrink SOT). TR-PDSO-G.	2013	JEDEC	0
417	MO-207N	Registration - Square and Rectangular Die-Size, Ball Grid Array Family. (L, T, V, W) F (R)- xDSB.	2013	JEDEC	0
418	MO-304D	Registration - Ball Grid Array Family, Rectangular, 1.0 mm pitch. (V, T, L) R-PBGA	2013	JEDEC	0
419	MO-305C	Registration - Wide I/O Micropillar Grid Array Package (MPGA) (X2,X3,X4)F(R)-SCDS	2013	JEDEC	0
420	MO-312A	Registration - 4 Lead Flat and Gullwing Surface Mount Power Package. HB1-PDSO, HB1-PSOF	2013	JEDEC	0
421	PRN13-NM1	PRELIMINARY RELEASE FOR JESD21: DDR3 MINI-UDIMM RC F0(x8 2R, STACKED)	2013	JEDEC	0
422	PRN13-NM3	PRELIMINARY RELEASE FOR JESD21: DDR3 MINI-RDIMM ANNEX D (x8 2R, Planar)	2013	JEDEC	0
423	SPP-023B	Standard Practices and Procedures - Module Insertion Procedure for DIMM and miniDIMM Connectors	2013	JEDEC	0
424	TO-263F	Registration - Plastic Surface Mounted Header Family. H-PSIP-G.	2013	JEDEC	0
425	JESD84-B50	Embedded Multi-Media Card (e MMC) Electrical Standard (5.0)	2013	JEDEC	0
426	MO-308A	Registration - Thick Thermally Enhanced Fine Pitch Square Ball Grid Array Family. BF-XBGA	2012	JEDEC	0
427	SO-008B	Registration - DDR1/DDR2/DDR3, 144 Pin, 16b/32b Small Outline Dual Inline Memory Module (SODIMM), 0.8 mm Pitch, Socket Outline.	2012	JEDEC	0
428	MO-303B	Registration - Land Grid Array Family, Rectangular, 0.50 mm Pitch	2012	JEDEC	0
429	MO-296B	Registration - Scalable Quad Flat No-lead Packages, Square and Rectangular. H-PQFN, HL-PQFN.	2012	JEDEC	0
430	MO-229F	Registration - Thermally Enhanced Plastic Very Thin, Very Very Thin, and Ultra Thin Fine Pitch Small Outline No Lead Package Family. H(V, W, U)F-PSON	2012	JEDEC	0
431	MO-240C	Registration - Thermally Enhanced, 8 Lead, 1.27 & 0.65 mm Pitch, Thin, Very Very thin, and Ultra Thin Plastic Dual Flat, No Lead Package. H(T, W, U)-PSON.	2012	JEDEC	0
432	MO-244D	Registration - 244 Pin DDR2/DDR3 Mini Dual-In-Line Memory Module (DIMM) Family, 0.60 mm Lead Centers.	2012	JEDEC	0
433	JESD99C	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES:	2012	JEDEC	0
434	JESD84-B451	Embedded Multimedia Card (e MMC) Electrical Standard 4.51	2012	JEDEC	0

435	JESD79-3F	DDR3 SDRAM STANDARD	2012	JEDEC	0
436	JESD77D	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES	2012	JEDEC	0
437	JESD51-50	OVERVIEW OF METHODOLOGIES FOR THE THERMAL MEASUREMENT OF SINGLE- AND MULTI-CHIP, SINGLE- AND MULTI-PN-JUNCTION LIGHT-EMITTING DIODES (LEDS)	2012	JEDEC	0
438	JESD51-51	IMPLEMENTATION OF THE ELECTRICAL TEST METHOD FOR THE MEASUREMENT OF REAL THERMAL RESISTANCE AND IMPEDANCE OF LIGHT-EMITTING DIODES WITH EXPOSED COOLING SURFACE	2012	JEDEC	0
439	JESD51-52	GUIDELINES FOR COMBINING CIE 127-2007 TOTAL FLUX MEASUREMENTS WITH THERMAL MEASUREMENTS OF LEDS WITH EXPOSED COOLING SURFACE	2012	JEDEC	0
440	JESD51-53	TERMS, DEFINITIONS AND UNITS GLOSSARY FOR LED THERMAL TESTING	2012	JEDEC	0
441	JESD671B	COMPONENT QUALITY PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS (INCLUDING ADMINISTRATIVE QUALITY PROBLEMS)	2012	JEDEC	0
442	JESD51-12.01	GUIDELINES FOR REPORTING AND USING ELECTRONIC PACKAGE THERMAL INFORMATION	2012	JEDEC	0
443	JESD211.01	ZENER AND VOLTAGE REGULATOR DIODE RATING VERIFICATION AND CHARACTERIZATION TESTING	2012	JEDEC	0
444	JESD219A	SOLID-STATE DRIVE (SSD) ENDURANCE WORKLOADS	2012	JEDEC	0
445	JESD204B.01	SERIAL INTERFACE FOR DATA CONVERTERS	2012	JEDEC	0
446	JEP155A.01	RECOMMENDED ESD TARGET LEVELS FOR HBM/MM QUALIFICATION	2012	JEDEC	0
447	JEP131B	POTENTIAL FAILURE MODE AND EFFECTS ANALYSIS (FMEA)	2012	JEDEC	0
448	JEP143C	SOLID STATE RELIABILITY ASSESSMENT QUALIFICATION METHODOLOGIES:	2012	JEDEC	0
449	J-STD-033C	JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING, AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES	2012	JEDEC	0
450	JS9704A	IPC/JEDEC-9704A: PRINTED WIRING BOARD (PWB) STRAIN GAGE TEST GUIDELINE	2012	JEDEC	0
451	MODULE4.20.23	240-Pin, 72 bit-wide, PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification	2012	JEDEC	0
452	MODULE4.20.22.C	144-Pin EP3-3200/EP3-4200/EP3-5300/EP3-6400 Unbuffered 32b-SO-DIMM Design Specification	2012	JEDEC	0
453	MODULE4.20.22	144-Pin EP3-3200/EP3-4200/EP3-5300/EP3-6400 Unbuffered 32b-SO-DIMM Design Specification	2012	JEDEC	0
454	MODULE4.20.22.A	144-Pin EP3-3200/EP3-4200/EP3-5300/EP3-6400 Unbuffered 32b-SO-DIMM Design Specification	2012	JEDEC	0
455	MODULE4.20.20.L	Annex L, R/C L, in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification. Item 2145.13B	2012	JEDEC	0
456	MODULE4.20.21	204-Pin EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM 72b-S0-DIMM Design Specification	2012	JEDEC	0
457	MODULE4.20.20.N	Annex N, R/C N, in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification. Item 2145.22	2012	JEDEC	0
458	MODULE4.20.20.U	R/C U, in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification	2012	JEDEC	0
459	MODULE4.20.20	240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification	2012	JEDEC	0
460	MODULE4.20.13	240-Pin PC2-5300/PC2-6400 DDR2 SDRAM Unbuffered DIMM Design Specification	2012	JEDEC	0
461	JESD22-B113A	BOARD LEVEL CYCLIC BEND TEST METHOD FOR INTERCONNECT RELIABILITY CHARACTERIZATION OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS	2012	JEDEC	0
462	MCP3.12.2	Package-on-Package (PoP) and Internal Stacked Module (ISM)	2012	JEDEC	0
463	SPD4.1.4	Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor.	2011	JEDEC	0

464	MODULE4.8	DDR3 240-Pin Connector S-Parameters Specification	2011	JEDEC	0
465	JESD22-B114A	MARK LEGIBILITY	2011	JEDEC	0
466	JESD22-B118	SEMICONDUCTOR WAFER AND DIE BACKSIDE EXTERNAL VISUAL INSPECTION	2011	JEDEC	0
467	JESD22-B107D	MARKING PERMANENCY	2011	JEDEC	0
468	JESD22-B105D	LEAD INTEGRITY	2011	JEDEC	0
469	JESD22-A109B	HERMETICITY	2011	JEDEC	0
470	JESD22-A117C	ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST	2011	JEDEC	0
471	MODULE4.20.20.E	Annex E, R/C E in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification	2011	JEDEC	0
472	MODULE4.20.20.F	Annex F, R/C F in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification	2011	JEDEC	0
473	MODULE4.20.20.AB	Annex AB, R/C AB in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification	2011	JEDEC	0
474	MODULE4.20.20.A	Annex A, R/C A in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification	2011	JEDEC	0
475	MODULE4.20.20.B	Annex B, R/C B in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification	2011	JEDEC	0
476	MODULE4.20.20.C	Annex C, R/C C in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification	2011	JEDEC	0
477	MODULE4.20.20.V	Annex V, R/C V in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification	2011	JEDEC	0
478	MODULE4.20.20.J	Annex J, R/C J in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification.	2011	JEDEC	0
479	MODULE4.20.20.K	Annex K, R/C K in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800/PC3-14900/PC3-17000 DDR3 SDRAM Registered DIMM Design Specification (1Rx8 VLP).	2011	JEDEC	0
480	MODULE4.20.21.A	204-Pin EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM 72b-SODIMM Design Specification	2011	JEDEC	0
481	MODULE4.20.21.B	204-Pin EP3-6400/EP3-8500/EP3-10600/EP3-12800 DDR3 SDRAM 72b-SO-DIMM Design Specification	2011	JEDEC	0
482	DR-4.22C.02	Design Requirements - Fine-pitch, Square Ball Grid Array Package (FBGA) Package-on-Package (PoP).	2011	JEDEC	0
483	JEP144A	GUIDELINE FOR INTERNAL GAS ANALYSIS FOR MICROELECTRONIC PACKAGES	2011	JEDEC	0
484	JEP160	LONG-TERM STORAGE GUIDELINES FOR ELECTRONIC SOLID-STATE WAFERS, DICE, AND DEVICES	2011	JEDEC	0
485	JEP161	SYSTEM LEVEL ESD PART 1: COMMON MISCONCEPTIONS AND RECOMMENDED BASIC APPROACHES	2011	JEDEC	0
486	JESD221	ALPHA RADIATION MEASUREMENT IN ELECTRONIC MATERIALS	2011	JEDEC	0
487	JESD229	WIDE I/O SINGLE DATA RATE (WIDE I/O SDR)	2011	JEDEC	0
488	JESD625B	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES	2011	JEDEC	0
489	JESD79-3-2	Addendum No. 2 to JESD79-3 - 1.25 V DDR3U-800, DDR3U-1066, DDR3U-1333, and DDR3U-1600	2011	JEDEC	0
490	JIG-101 Ed. 4.0	MATERIAL COMPOSITION DECLARATION FOR ELECTRONIC PRODUCTS	2011	JEDEC	0
491	MO-220-K.01	Registration - Thermally Enhanced Plastic Very Thin and Very Very Thin Fine Pitch Quad Flat No Lead Package. HVF-PQFN, HWF-QFN.	2011	JEDEC	0
492	JESD8-24	POD12 ? 1.2 V PSEUDO OPEN DRAIN INTERFACE	2011	JEDEC	0
493	JESD8-25	POD10-1.0 V PSUEDO OPEN DRAIN INTERFACE	2011	JEDEC	0
494	JESD8-26	1.2 V HIGH-SPEED LVCMOS (HS LVCMOS) INTERFACE	2011	JEDEC	0
495	MO-237-G.01	Registration - DDR2 SDRAM DIMM (Dual Inline Memory Module) Family with 1.00 mm Contact Centers.	2011	JEDEC	0

496	MO-306A	Registration - Flange Mounted Family Surface Mount (Peripheral Terminals). HR-PSFM-G.	2011	JEDEC	0
497	MO-307A	Registration - Dual-Pitch, rectangular Ball Grid Array package, 0.50 mm x 0.65 mm Pitch. LFR-XBGA	2011	JEDEC	0
498	MO-275-A.01	Registration - Low profile, Fine Pitch Ball Grid Array Family, Square. LF-XBGA. Item 11.11-751E.	2011	JEDEC	0
499	MO-273C	Registration - Upper PoP Package, Square, Fine Pitch, Ball Grid Array (BGA), 0.65 and 0.50 mm and 0.40 mm Pitch. POP-XFBGA.	2011	JEDEC	0
500	SO-015A	Registration - mSATA SSD 0.80 mm Pitch Socket Outline. SKT	2011	JEDEC	0
501	PRN11-NM1	DDR3 Unbuffered Mini-DIMM, Annex A	2011	JEDEC	0
502	PRN11-NM2	DDR3 Unbuffered Mini-DIMM, Annex B	2011	JEDEC	0
503	TO-281A	Registration - Fully Molded Flange Header Family, Full-Pak. B2E-PSIP-F	2011	JEDEC	0
504	TO-280-A	Registration - Flange Mounted Header Family. H-PSOF	2010	JEDEC	0
505	MO-301A	Registration - Standard and Low, Fine Pitch Rectangular Ball Grid Array Family, 0.65 mm Pitch. FR-XBGA, LFR-XBGA.	2010	JEDEC	0
506	MO-292C	Registration - Very Thin Fine Pitch Plastic Quad Flat Package, 2.00 mm Footprint (Staggered Dual Row). HVF-PQFP.	2010	JEDEC	0
507	MO-236C	Registration - Plastic, Ultra and Super Thin, Small Outline, No Lead Package. (U, X2) F-PSON.	2010	JEDEC	0
508	MO-252D	Registration - Plastic Very Very Thin, Ultra Thin and Extremely Thin, Fine Pitch Dual, Small Outline, Non-leaded Package Family. (W, U, X)F-PSON.	2010	JEDEC	0
509	JESD84-A441	EMBEDDED MULTIMEDIACARD(e_MMC) e_MMC/CARD PRODUCT STANDARD, HIGH CAPACITY, including Reliable Write, Boot, Sleep Modes, Dual Data Rate, Multiple Partitions Supports, Security Enhancement, Background Operation and High Priority Interrupt (MMCA, 4.41)	2010	JEDEC	0
510	JESD82-29A	DEFINITION OF THE SSTE32882 REGISTERING CLOCK DRIVER WITH PARITY AND QUAD CHIP SELECTS FOR DDR3/DDR3L/DDR3U RDIMM 1.5 V/1.35 V/1.25 V APPLICATIONS	2010	JEDEC	0
511	MO-222-B.01	Registration - Very Thin Profile, Fine Pitch, Bump Grid Array Family, 0.50 & 0.65 mm Pitch, Rectangular. VFR-XBGA.	2010	JEDEC	0
512	MO-203C	Registration - Plastic Thin Shrink Small Outline (Shrink SOT). R-PDSO-G	2010	JEDEC	0
513	MO-187-F	Registration - Plastic Low/Thin/Very Thin Shrink Small Outline Package, 0.65 AND 0.50 Pitch. (H)(L,T,V)SR-PDSO.	2010	JEDEC	0
514	JM7.01	STYLE MANUAL FOR STANDARDS AND OTHER PUBLICATIONS OF JEDEC	2010	JEDEC	0
515	MO-137E	Registration - Plastic Shrink Small Outline Package (SSOP) Family. R-PDSO/SSOP/SOIC.	2010	JEDEC	0
516	JESD51-14	TRANSIENT DUAL INTERFACE TEST METHOD FOR THE MEASUREMENT OF THE THERMAL RESISTANCE JUNCTION-TO-CASE OF SEMICONDUCTOR DEVICES WITH HEAT FLOW THROUGH A SINGLE PATH	2010	JEDEC	0
517	JESD51-32	EXTENSION TO JESD51 THERMAL TEST BOARD STANDARDS TO ACCOMMODATE MULTI-CHIP PACKAGES	2010	JEDEC	0
518	JESD209B	LOW POWER DOUBLE DATA RATE (LPDDR) SDRAM STANDARD	2010	JEDEC	0
519	JEP133C	GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS:	2010	JEDEC	0
520	MODULE4.20.10	240-Pin PC2-6400/PC2-5300/PC2-4200/PC2-3200 DDR2 SDRAM Registered DIMM Design Standard, Rev 4.04.	2010	JEDEC	0
521	JESD22-A111A	EVALUATION PROCEDURE FOR DETERMINING CAPABILITY TO BOTTOM SIDE BOARD ATTACH BY FULL BODY SOLDER IMMERSION OF SMALL SURFACE MOUNT SOLID STATE DEVICES:	2010	JEDEC	0
522	JESD22-B108B	COPLANARITY TEST FOR SURFACE-MOUNT SEMICONDUCTOR DEVICES	2010	JEDEC	0
523	SPD4.1.TOC	Serial Presence Detect (SPD) Table of Contents	2010	JEDEC	0
524	SPD4.1.5	TS3000 Standalone Thermal Sensor Component	2009	JEDEC	0
525	SPD4.1.3	Definition of the EE1002 and EE1002A Serial Presence Detect (SPD) EEPROMs	2009	JEDEC	0
526	JESD22-B112A	PACKAGE WARPAGE MEASUREMENT OF SURFACE-MOUNT INTEGRATED CIRCUITS AT ELEVATED TEMPERATURE	2009	JEDEC	0
527	NVRAM3.6.3	Low Power Double Data Rate (LPDDR) Non-Volatile Memory (NVM) (Item 1674.17, 1674.16, 1674.20	2009	JEDEC	0

528	MODULE4.20.20.G	Annex G, R/C G, in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification. Item 2082.24B	2009	JEDEC	0
529	MODULE4.20.20.H	Annex H, R/C H, in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification. Item 2156.08	2009	JEDEC	0
530	MODULE4.20.20.D	Annex D, R/C D, in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification. Item 2082.22B	2009	JEDEC	0
531	MODULE4.20.20.M	Annex M, R/C M, in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification. Item 2145.06A	2009	JEDEC	0
532	MODULE4.20.20.W	Annex W, R/C W, in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification. Item 2156.07	2009	JEDEC	0
533	MODULE4.20.20.Y	Annex Y, R/C Y, in 240-Pin PC3-6400/PC3-8500/PC3-10600/PC3-12800 DDR3 SDRAM Registered DIMM Design Specification. Item 2156.06	2009	JEDEC	0
534	JEP146A	GUIDELINES FOR SUPPLIER PERFORMANCE RATING:	2009	JEDEC	0
535	JEP156	CHIP-PACKAGE INTERACTION UNDERSTANDING, IDENTIFICATION AND EVALUATION	2009	JEDEC	0
536	JEP157	RECOMMENDED ESD-CDM TARGET LEVELS	2009	JEDEC	0
537	JEP158	3D CHIP STACK WITH THROUGH-SILICON VIAS (TSVS): Identifying, Evaluating and Understanding Reliability Interactions	2009	JEDEC	0
538	JS9703	IPC/JEDEC-9703: MECHANICAL SHOCK TEST GUIDELINE FOR SOLDER JOINT RELIABILITY	2009	JEDEC	0
539	GS-009A	Standard - SMT DDR3 DIMM Socket Coplanarity Measurement Gauge. Item 11.14-124.	2009	JEDEC	0
540	JESD209A-1	Addendum No. 1 to JESD209A - LOW POWER DOUBLE DATA RATE (LPDDR) SDRAM, 1.2 V I/O.	2009	JEDEC	0
541	JESD51-13	GLOSSARY OF THERMAL MEASUREMENT TERMS AND DEFINITIONS	2009	JEDEC	0
542	JESD79-2F	DDR2 SDRAM STANDARD	2009	JEDEC	0
543	JESD84-A44	EMBEDDED MULTIMEDIACARD(e·MMC) e·MMC/CARD PRODUCT STANDARD, HIGH CAPACITY, Including Reliable Write, Boot, Sleep Modes, Dual Data Rate, Multiple Partitions Supports and Security Enhancement (MMCA, 4.4) - SUPERSEDED BY JESD84-A441, March 2010	2009	JEDEC	0
544	JESD84-C44	EMBEDDED MULTIMEDIACARD (e·MMC) MECHANICAL STANDARD, WITH OPTIONAL RESET SIGNAL	2009	JEDEC	0
545	JESD86A	ELECTRICAL PARAMETERS ASSESSMENT	2009	JEDEC	0
546	JESD8-20A	POD15 - 1.5 V PSEUDO OPEN DRAIN I/O	2009	JEDEC	0
547	JESD8-23	UNIFIED WIDE POWER SUPPLY VOLTAGE RANGE CMOS DC INTERFACE STANDARD FOR NON-TERMINATED DIGITAL INTEGRATED CIRCUITS	2009	JEDEC	0
548	JESD82-20A	FBDIMM: ADVANCED MEMORY BUFFER (AMB)	2009	JEDEC	0
549	MO-288-B	Registration - Small Scale, Plastic, Ultra, Extra, and Super Thin, Fine Pitch, Quad Flat No Lead Package (with Optional Thermal Enhancements). (U, X1, X2)F-PQFN & H(U, X1, X2)F-PQFN.	2009	JEDEC	0
550	MO-297-A	Registration - Slim Lite SSD Assembly. DIM.	2009	JEDEC	0
551	MO-298-A	Registration - Thin, Very-Thin, Very-Very-Thin Profile, Fine Pitch Ball Grid Array Family, 0.40mm pitch (Square). (T,V,W)F-XBGA.	2009	JEDEC	0
552	MO-295-A	Registration - Thin Profile, Interstitial Fine Pitch Ball Grid Array Family, Square. TFI-PBGA.	2009	JEDEC	0
553	PRN09-NM4	DDR3 DIMM Label	2009	JEDEC	0
554	PRN09-NV2	TSE2002 Serial Presence Detect with Thermal Sensor	2009	JEDEC	0
555	SPP-024A	Standard Practices and Procedures - Reflow Flatness Requirements for Ball Grid Array Packages. Item 11.2-783	2009	JEDEC	0
556	TO-270C	Registration - 2 and 4 Lead Surface Mount Power Package. (H,HB1)-PDSO, (H,HB1)-PSOF. Item 11.10-446.	2008	JEDEC	0
557	TO-279B	Registration - Plastic Surface Mounted Header Family. R-PSFM-F. Item 11.10-447.	2008	JEDEC	0
558	MS-012F	Standard - Plastic Small Outline (SO) Family Peripheral Terminals, 1.27 mm Pitch, 3.90 mm Body Width (Mold Flash and End Protrusion). R-PDSO/SOP/SOIC. Item 11.11-801(s).	2008	JEDEC	0
559	SO-007B	Registration - DDR3 DIMM 240 Position Socket Outline, 1.00 mm Contact centers	2008	JEDEC	0

560	SO-014A	Registration - DDR3 DIMM 240 Pin SMT Socket Outline with 1.00 mm Contact Centers. SKT. Item 11.14-123	2008	JEDEC	0
561	MO-291-B	Registration - Very Thin Fine Pitch Plastic Quad Flat Package, 2.00 mm Footprint. HVF-PQFP.	2008	JEDEC	0
562	MO-293-A	Registration - Plastic, ultra, Extra and Super Thin, Fine Pitch, Dual Small Outline, Flat, Leaded Package. (U, X1, X2)F-PSOF, HX2-PSOF.	2008	JEDEC	0
563	MO-294-A	Registration - Very Thin Profile, Fine Pitch, Square Bump Grid Array Family. VF-XBGA.	2008	JEDEC	0
564	MO-283-B	Registration - Plastic Super Thin and Die Thin Profiles for RFID Dipole Straps. (X2, X4)-PUCD.	2008	JEDEC	0
565	MO-270-B	Registration - Extra Thin Profile, Fine Pitch, Internal Stacking Module (ISM) with Single Interconnect Array (0.75/0.80 mm Pitch, Square, Rectangular). X1F-XLGA.	2008	JEDEC	0
566	MO-253-B	Registration - 14 & 16 Lead Screw Mount and Surface Mount Power Package. HB1-PDSO/HB1-PSOF. Item 11.11-787	2008	JEDEC	0
567	MO-242-C	Registration - Rectangular Die-Size, Stacked Ball Grid Array Family, 0.80 mm Pitch. AF1R-PDSB.	2008	JEDEC	0
568	JESD8-18A	FBDIMM SPECIFICATION: HIGH SPEED DIFFERENTIAL PTP LINK AT 1.5 V	2008	JEDEC	0
569	JESD22-A114F	ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM)	2008	JEDEC	0
570	JESD82-28A	FULLY BUFFERED DIMM DESIGN FOR TEST, DESIGN FOR VALIDATION (DFx)	2008	JEDEC	0
571	JM19.03	FILE NAMING CONVENTION:	2008	JEDEC	0
572	JESD79F	DOUBLE DATA RATE (DDR) SDRAM STANDARD	2008	JEDEC	0
573	JESD51-31	THERMAL TEST ENVIRONMENT MODIFICATIONS FOR MULTICHIP PACKAGES	2008	JEDEC	0
574	JESD50B.01	SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION AND OUTLIER MANAGEMENT	2008	JEDEC	0
575	JESD201A	ENVIRONMENTAL ACCEPTANCE REQUIREMENTS FOR TIN WHISKER SUSCEPTIBILITY OF TIN AND TIN ALLOY SURFACE FINISHED	2008	JEDEC	0
576	JESD15-1	COMPACT THERMAL MODEL OVERVIEW	2008	JEDEC	0
577	JESD15-3	TWO-RESISTOR COMPACT THERMAL MODEL GUIDELINE	2008	JEDEC	0
578	JESD15-4	DELPHI COMPACT THERMAL MODEL GUIDELINE	2008	JEDEC	0
579	JESD15	THERMAL MODELING OVERVIEW	2008	JEDEC	0
580	JEP154	GUIDELINE FOR CHARACTERIZING SOLDER BUMP ELECTROMIGRATION UNDER CONSTANT CURRENT AND TEMPERATURE STRESS	2008	JEDEC	0
581	MODULE4.20.11	200-Pin DDR2 SDRAM Unbuffered SODIMM Design Specification	2008	JEDEC	0
582	DG-4.17C	Design Requirements - Ball Grid Array (BGA)Package Measuring and Methodology.	2008	JEDEC	0
583	JESD21C.6	JESD21C, Section 6, Applicable other documents for JESD21C	2008	JEDEC	0
584	SRAM3.7.10	High Speed DDR SRAM in 165 BGA	2008	JEDEC	0
585	SDRAM3.11.4	Word Wide SDRAM.	2008	JEDEC	0
586	JESD22-A121A	MEASURING WHISKER GROWTH ON TIN AND TIN ALLOY SURFACE FINISHES	2008	JEDEC	0
587	SPD4.1.2	SPD General Standard.	2008	JEDEC	0
588	SDRAM3.11.5.5	DDR2 Specific SDRAM Function	2008	JEDEC	0
589	SPD4.1.2.10	SPD Annex J: Serial Presence Detect for DDR2 SDRAM	2007	JEDEC	0
590	SRAM3.7.7	Word Wide TTL and MOS SRAM	2007	JEDEC	0
591	SRAM3.7.8	Double Word Wide MOS SRAM	2007	JEDEC	0
592	SRAM3.7.9	Eight Byte Wide (X64/72) MOS SRAM	2007	JEDEC	0
593	PSRAM3.8	PSRAM, Pseudo-Static RAM	2007	JEDEC	0
594	EEPROM3.5.2	EEPROM, Word Wide	2007	JEDEC	0
595	DG-4.21A	Design Requirements - Internal Stacking Module, Land Grid Array Packages with External Interconnect Terminals (ISM).	2007	JEDEC	0

596	DG-4.19D	Design Requirements - Quad No-Lead Staggered and Inline Multi-Row Packages (with optional thermal enhancements). QFN.	2007	JEDEC	0
597	MODULE4.20.16	144-Pin EP2-2100 DDR2 SDRAM 32b S0DIMM Design Specification, Rev 1.0. Item 2043.09.	2007	JEDEC	0
598	MODULE4.20.17	DDR3 Unbuffered MicroDIMM Design Specification, 214-Pin PC3-12800. Item 2031.04	2007	JEDEC	0
599	JEP152	DDR2 DIMM CLOCK SKEW MEASUREMENT PROCEDURE USING A CLOCK REFERENCE BOARD	2007	JEDEC	0
600	GS-006-A	Standard - SMT DDR2 DIMM Socket, Coplanarity Measurement Gauge. Item 11.14-102.	2007	JEDEC	0
601	GS-007-A	Standard - DDR2 DIMM Socket Insertion and Extraction Force Gauge. Item 11.14-103.	2007	JEDEC	0
602	GS-008-A	Registration - DDR3 DIMM Connector Insertion Force Gauge. Item 11.14-110.	2007	JEDEC	0
603	JEP114.01	GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION	2007	JEDEC	0
604	JESD205	FBDIMM STANDARD: DDR2 SDRAM FULLY BUFFERED DIMM (FBDIMM) DESIGN STANDARD	2007	JEDEC	0
605	JESD206	FBDIMM ARCHITECTURE AND PROTOCOL	2007	JEDEC	0
606	JESD207	RADIO FRONT END - BASEBAND DIGITAL PARALLEL (RBDP) INTERFACE	2007	JEDEC	0
607	JESD208	SPECIALITY DDR2-1066 SDRAM	2007	JEDEC	0
608	JESD51-2A	INTEGRATED CIRCUITS THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - NATURAL CONVECTION (STILL AIR)	2007	JEDEC	0
609	JESD8-11A.01	ADDENDUM No. 11A.01 to JESD8 - 1.5 V +/- 0.1 V (NORMAL RANGE) AND 0.9 - 1.6 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:	2007	JEDEC	0
610	JESD8-12A.01	1.2 V +/- 0.1 V (NORMAL RANGE) AND 0.8 - 1.3 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:	2007	JEDEC	0
611	JESD8-14A.01	1.0 V +/- 0.1 V (NORMAL RANGE) AND 0.7 V - 1.1 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:	2007	JEDEC	0
612	JESD74A	EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR SEMICONDUCTOR COMPONENTS:	2007	JEDEC	0
613	JESD69B	INFORMATION REQUIREMENTS FOR THE QUALIFICATION OF SILICON DEVICES	2007	JEDEC	0
614	JESD61A.01	ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE:	2007	JEDEC	0
615	JESD96A-1	Addendum 1 to JESD96A - INTEROPERABILITY AND COMPLIANCE TECHNICAL REQUIREMENTS FOR JEDEC STANDARD JESD96A - RECOMMENDED PRACTICE FOR USE WITH IEEE 802.11N	2007	JEDEC	0
616	MO-225-C	Registration - Very Thin, Fine-Pitch, Square Ball Grid Array Family, 0.50/0.65 mm pitch. VF-XBGA.	2007	JEDEC	0
617	MO-219-G	Registration - Low Profile, Fine Pitch, Ball Grid Array (FBGA) Registration, 0.80 mm pitch (Square and Rectangle). LF-XBGA, LFR-XBGA.	2007	JEDEC	0
618	JESD82-9B	DEFINITION OF SSTU32865 REGISTERED BUFFER WITH PARITY FOR 2R x 4 DDR2 RDIMM APPLICATIONS	2007	JEDEC	0
619	JESD84-A41	EMBEDDED MULTIMEDIACARD (e·MMC) PRODUCT STANDARD, STANDARD CAPACITY	2007	JEDEC	0
620	JESD84-A42	EMBEDDED MULTIMEDIACARD (e·MMC) PRODUCT STANDARD, HIGH CAPACITY	2007	JEDEC	0
621	JESD84-A43	EMBEDDED MULTIMEDIACARD (e·MMC) e·MMC/CARD PRODUCT STANDARD, HIGH CAPACITY, INCLUDING RELIABLE WRITE, BOOT, AND SLEEP MODES (MMCA, 4.3)	2007	JEDEC	0
622	JESD82-23	DEFINITION OF the SSTUA32S869 AND SSTUA32D869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS	2007	JEDEC	0
623	JESD82-24	DEFINITION OF the SSTUB32865 28-bit 1:2 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS	2007	JEDEC	0
624	JESD82-25	DEFINITION OF the SSTUB32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS	2007	JEDEC	0
625	JESD82-26	DEFINITION OF THE SSTUB32868 REGISTERED BUFFER WITH PARITY FOR 2R x 4 DDR2 RDIMM APPLICATIONS	2007	JEDEC	0

626	JESD82-27	DEFINITION OF THE SSTUB32869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS:	2007	JEDEC	0
627	JESD89-1A	TEST METHOD FOR REAL-TIME SOFT ERROR RATE	2007	JEDEC	0
628	JESD89-2A	TEST METHOD FOR ALPHA SOURCE ACCELERATED SOFT ERROR RATE	2007	JEDEC	0
629	JESD89-3A	TEST METHOD FOR BEAM ACCELERATED SOFT ERROR RATE	2007	JEDEC	0
630	JESD84-C01	MULTIMEDIACARD (MMC) MECHANICAL STANDARD	2007	JEDEC	0
631	JESD84-C43	EMBEDDED MULTIMEDIACARD (e·MMC) MECHANICAL STANDARD	2007	JEDEC	0
632	JESD84-B41	MULTIMEDIACARD (MMC) ELECTRICAL STANDARD, STANDARD CAPACITY (MMCA, 4.1)	2007	JEDEC	0
633	JESD84-B42	MULTIMEDIACARD (MMC) ELECTRICAL STANDARD, HIGH CAPACITY (MMCA, 4.2)	2007	JEDEC	0
634	JESD8-3A	ADDENDUM No. 3A to JESD8 - GUNNING TRANSCEIVER LOGIC (GTL) LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:	2007	JEDEC	0
635	JESD8-5A.01	ADDENDUM No. 5 to JESD8 - 2.5 V 0.2 V (NORMAL RANGE), AND 1.8 V TO 2.7 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT	2007	JEDEC	0
636	JESD82-21	STANDARD FOR DEFINITION OF CUA845 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS	2007	JEDEC	0
637	JESD82-16A	DEFINITION OF THE SSTUA32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY TEST FOR DDR2 RDIMM APPLICATIONS	2007	JEDEC	0
638	JESD82-18A	STANDARD FOR DEFINITION OF THE CUA877 AND CU2A877 PLL CLOCK DRIVERS FOR REGISTERED DDR2 DIMM APPLICATIONS	2007	JEDEC	0
639	JESD82-19A	DEFINITION OF THE SSTUA32S865 AND SSTUA32D865 28-BIT 1:2 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS	2007	JEDEC	0
640	JESD82-10A	DEFINITION OF THE SSTU32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS	2007	JEDEC	0
641	JESD82-12A	DEFINITION OF THE SSTU32S869 AND SSTU32D869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS	2007	JEDEC	0
642	MO-247-D	Registration - Plastic, Quad, No-Lead, Staggered, Multi-Row Packages. H(V,W,U)F-PQFN.	2007	JEDEC	0
643	MO-256-F	Registration - FBDIMM (Fully Buffered Dual Inline Memory Module) Family, 1.00 mm Contact Centers.	2007	JEDEC	0
644	MO-284-A	Registration - Thin, Fine-Pitch, Rectangular Dual Pitch Ball Grid Array Family, 0.80 mm x 1.00 mm pitch. TFR-XBGA.	2007	JEDEC	0
645	MO-285-A	Registration - Very Thin, Fine-Pitch, Rectangular, Ball Grid Array Family, 0.50/0.65/0.80 mm pitch. VFR-XBGA.	2007	JEDEC	0
646	MO-287-A	Registration - Small Scale, Plastic, Ultra, Extra, and Super Thin, Fine Pitch, Dual Small Outline, No Lead Package. (U, X1, X2)F-PSON.	2007	JEDEC	0
647	MO-282-A	Registration - FBDIMM (Dual In-Line Memory Module) Family, Flex-Based, 1.00 mm Contact Centers.	2007	JEDEC	0
648	MO-290-A	Registration - DDR3 SDRAM DIMM (Dual Inline Memory Module) Family, Flex-Based, 1.00 mm contact Centers	2007	JEDEC	0
649	SO-006B	Registration - 204 Pin SO-DDR3 SDRAM, 0.60 mm Contact Centers, Socket Outline.	2007	JEDEC	0
650	SO-009A	Registration - DDR2 DIMM 240 Pin SMT Socket Outline with 1.00 mm Contact Centers. Item 11.14-097.	2007	JEDEC	0
651	SO-011A	Registration - 240 Pin DDR2 DIMM 1.00 mm Contact Centers, Press Fit Socket Outline. Item 11.14-111	2007	JEDEC	0
652	SO-012A	Registration - 240 Pin DDR3 DIMM 1.00 mm Contact Centers, Press Fit Socket Outline.	2007	JEDEC	0
653	SO-013A	Registration - 240 Pin FBDIMM 1.00 mm Contact Centers, Press Fit Socket Outline. SKT. Item 11.14-113	2007	JEDEC	0
654	PS-001A	Performance Standard - 240 Pin DDR3, UDIMM. Item 11.14-109(S)	2007	JEDEC	0
655	TO-272-C	Registration - 2, 4, and 6 Lead Screw Mount Power Package. PDFP-(C, F, G). Item 11.10-444.	2007	JEDEC	0
656	SPP-021A	Standard Practices and Procedures - Change Record Methodology. Item 11.2-710(S)	2006	JEDEC	0
657	SPP-022B	Standard Practices and Procedures - Thermal Pad Requirements. Item 11.2-748(S)	2006	JEDEC	0
658	TO-277A	Registration - Small Outines Plastic Surface Mount Package. T-PSON-3. Item 11.10-436	2006	JEDEC	0
659	TO-278B	Registration - Thin profile, 3 lead, Plastic Small Outline, Surface Mount. T-PSOF-3. Item 11.10-441(E).	2006	JEDEC	0
660	SO-003B	Registration - FBDIMM, 240 Position Socket Outline with 1.00 mm Contact Centers. Item 11.14-082 and 11.14-087.	2006	JEDEC	0

661	SPP-003C	Standard Practices and Procedures - Metrication.	2006	JEDEC	0
662	MO-271-A	Registration - Small outline packages (7.60 mm body width) with an exposed pad. (F)-PDSO / SOIC, SOP.	2006	JEDEC	0
663	MO-272-A	Registration - Low profile, Exposed pads, Plastic Small Outline Family, with 3.90 mm Body Size. (F) L-PDSO/SOIC, LSOP.	2006	JEDEC	0
664	MO-277-A	Registration - 13 Pin Full Size MultiMediaCard (MMC) Outline - MMCplus 32 x 24 x 1.4 mm. RL-PLGA/MMCplus.	2006	JEDEC	0
665	MO-278-A	Registration - 13 Pin Reduced Size MultiMediaCard (MMC) Outline - MMCmobile 18 x 24 x 1.4 mm. RL-PLGA/MMCmobile.	2006	JEDEC	0
666	MO-279-A	Registration - 10 Pin Micro Size MultiMediaCard (MMC) Outline - MMCmicro 14 x 12 x 1.1 mm. RT-PLGA/MMCmicro.	2006	JEDEC	0
667	MO-280-A	Registration - Ultra Thin and Very, Very Thin Profile, Fine Pitch Ball Grid Array (BGA) Family - SQUARE. (U,W)F-XBGA.	2006	JEDEC	0
668	MO-281-A	Registration - DDR2 SDRAM DIMM (Dual Inline memory Module) Family, Flex-Based, 1.00 mm Contact Centers.	2006	JEDEC	0
669	MO-267-B	Registration - Punch-Singulated, Fine Pitch, Square, Very Thin, Leadframe-Based Quad No-Lead Staggered Dual-Row (With Optional Thermal Enhancements) QFN Package Family. HVF-PQFN.	2006	JEDEC	0
670	MO-260-C	Registration - DDR and DDR2 Micro DIMM Mezzanine, 214 pin, 0.4 mm Lead Centers.	2006	JEDEC	0
671	MO-248-E	Registration - Thermally Enhanced Plastic Ultra Thin and Extremely Thin Fine Pitch Quad Flat No Lead Package. H(U,X1)F-PQFP.	2006	JEDEC	0
672	JESD82-14A	DEFINITION OF THE SSTUB32868 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS	2006	JEDEC	0
673	JESD82-22	INSTRUMENTATION CHIP DATA SHEET FOR FBDIMM DIAGNOSTIC SENSELINES	2006	JEDEC	0
674	JESD8-7A	ADDENDUM No. 7 to JESD8 - 1.8 V + -0.15 V (NORMAL RANGE), AND 1.2 V - 1.95 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:	2006	JEDEC	0
675	JESD8-19	POD18 - 1.8 V PSEUDO OPEN DRAIN I/O	2006	JEDEC	0
676	JESD89A	MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES	2006	JEDEC	0
677	MO-224-E	Registration - 200 Pin DDR Small Outline Dual-In-Line Memory Module (SODIMM) Family, 0.60 mm Contact Centers. Item 11.14-077. Key tolerance corrected	2006	JEDEC	0
678	MO-195-D	Registration - Thin, Fine Pitch Ball Grid Array Family, 0.5 mm Pitch. TF(R)-XBGA.	2006	JEDEC	0
679	MO-205-G	Registration - Low Profile, Fine Pitch BGA Family, 0.80 mm Pitch (Rectangular). LFR-XBGA. Item 11.11-752.	2006	JEDEC	0
680	MO-206-E	Registration - Dual Inline Memory Module (DIMM) Family, 184 Pin DDR w/ 1.27 mm Contact Centers. Item 11.14-078	2006	JEDEC	0
681	JESD96A	RADIO FRONT END - BASEBAND (RF-BB) INTERFACE	2006	JEDEC	0
682	JP002	CURRENT TIN WHISKERS THEORY AND MITIGATION PRACTICES GUIDELINE	2006	JEDEC	0
683	JESD75-6	PSO-N/PQFN PINOUTS STANDARDIZED FOR 14-, 16-, 20-, AND 24-LEAD LOGIC FUNCTIONS:	2006	JEDEC	0
684	JESD202	METHOD FOR CHARACTERIZING THE ELECTROMIGRATION FAILURE TIME DISTRIBUTION OF INTERCONNECTS UNDER CONSTANT-CURRENT AND TEMPERATURE STRESS:	2006	JEDEC	0
685	JEP179	DDR2 SPD INTERPRETATION OF TEMPERATURE RANGE AND (SELF-) REFRESH OPERATION	2006	JEDEC	0
686	JEP121A	REQUIREMENTS FOR MICROELECTRONIC SCREENING AND TEST OPTIMIZATION:	2006	JEDEC	0
687	GS-004A	STANDARD - FBDIMM Socket Insertion and Extraction Force Gauge. Item 11.14-083(S)	2006	JEDEC	0
688	GS-005A	Standard - DDR3 DIMM Socket Insertion and Extraction Force Gauge. Item 11.14-098	2006	JEDEC	0
689	MODULE4.20.14	PC2-4200/PC2-3200 DDR2 Registered Mini-DIMM Design Specification Revision 2.0	2006	JEDEC	0
690	DG-4.8C	Design Requirements - Plastic Quad and Dual Inline, Square and Rectangular, No-Lead Packages (with Optional Thermal Enhancements). QFP-N/SO-N.	2006	JEDEC	0
691	DO-221A	Registration - Thin profile, Plastic Small Outline, Surface Mount. T-PSOF. Item 11.10-437.	2006	JEDEC	0
692	DO-222A	Registration - Very Thin, Small Outline Plastic Surface Mount Package. V-PSOF. Item 11.10-439.	2006	JEDEC	0
693	CO-035A	Registration - Thin Matrix Tray for Advanced Memory Buffer. Item 11.5-736.	2006	JEDEC	0

694	SPD4.1.2.9	SPD Annex I, Serial Presence Detect for Virtual Channel SDRAM, Revision 2	2006	JEDEC	0
695	SPD4.1.2.7	SPD Annex G, Serial Presence Detect for FBDIMM, Revision 1.1	2006	JEDEC	0
696	SDRAM3.11.5.8	Graphics Double Data (GDDR4) SGRAM Standard	2006	JEDEC	0
697	SDRAM3.11.5.TOC	SDRAM and SGRAM Architectural Operational Features Table of Contents	2006	JEDEC	0
698	MCP3.12.0	MCP Overview	2006	JEDEC	0
699	MCP3.12.3	Silicon Pad Sequence (x16/x32 LPDRAM, x16 PSRAM, x16 NAND). Item JC-63-029	2006	JEDEC	0
700	MODULE4.20.7	PC-2700/PC-3200 Registered DIMM Design Specification Revision 2.2	2006	JEDEC	0
701	MODULE4.7	Mobile Platform Memory Module Thermal Sensor Component Specification	2006	JEDEC	0
702	SDRAM3.11.5.6	GDDR2 Specific SGRAM Functions	2005	JEDEC	0
703	SDRAM3.11.5.7	GDDR3 Specific SGRAM Functions	2005	JEDEC	0
704	EEPROM3.5.3	EEPROM Extended Features	2005	JEDEC	0
705	EEPROM3.5.1	Byte Wide EEPROM	2005	JEDEC	0
706	DG-4.23A	Design Requirements - Punch-Singulated, Fine Pitch, Square, Very Thin and Very Very Thin Profile, Leadframe-Based Quad No-Lead Staggared Dual-Row Packages, (with optional Thermal Enhancements) QFN.	2005	JEDEC	0
707	JESD203	STANDARD TEST LOADS FOR DUAL-SUPPLY LEVEL TRANSLATION DEVICES	2005	JEDEC	0
708	JM5	JEDEC Legal Guides Manual	2005	JEDEC	0
709	JESD93	HYBRIDS/MCM	2005	JEDEC	0
710	MO-156-C	Registration - Square Ceramic Ball Grid Array (BGA) Family. 1.00, 1.27, and 1.50 mm pitch. CBGA. Item 11.10-432	2005	JEDEC	0
711	MO-157-C	Registration - Rectangular Ceramic Ball Grid Array (BGA) Family. CBGA. Item 11.10-433.	2005	JEDEC	0
712	JESD82-17	DEFINITION OF THE SSTUA32S868 AND SSTUA32D868 REGISTERED BUFFER WITH PARITY FOR 2R X 4 DDR2 RDIMM APPLICATIONS	2005	JEDEC	0
713	JESD82-15	STANDARD FOR DEFINITION OF CUA878 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS	2005	JEDEC	0
714	JESD82-13A	DEFINITION OF THE SSTVN16859 2.5-2.6 V 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR PC1600, PC2100, PC2700 AND PC3200 DDR DIMM APPLICATIONS	2005	JEDEC	0
715	MO-255-B	Registration - Plastic Very Very Thin, Ultra Thin, and Extremely Thin, Fine Pitch Quad Flat Small Outline, Non-Leaded Package Family. P-XFQFN. Item 11.11-678.	2005	JEDEC	0
716	MO-261-A	Registration - Thick and Very Thick, Fine-Pitch, Retangular Ball Grid Array Family, 0.80 mm Pitch. B1FR-XBGA, BFR-XBGA.	2005	JEDEC	0
717	MO-262-A	Registration - 0.50 mm pitch Very Thin and Very-Very Thin Flange-Molded Thermally Enhanced (Top Side) QFNs. HVF-PQFN, HWF-PQFN.	2005	JEDEC	0
718	MO-263-A	Registration - 0.50 and 0.40 mm pitch Very Thin and Very-Very Thin Flange-Molded QFNs. VF-PQFN, WF-PFQN.	2005	JEDEC	0
719	MO-264-A	Registration - Rectangular Die-Size, Stacked Ball Grid Array Family, Dual Pitch. AFR-PDSB.	2005	JEDEC	0
720	MO-265-A	Registration - Thermally Enhanced Plastic Very Thin Fine Pitch Quad Flat No Lead Package, includung Corner Terminals. HVF-PQFN.	2005	JEDEC	0
721	MO-259-A	48 Lead, Very, Very Thin Small Outline Package, Type 1. WR-PDSO1, WSOP1. Item 11.11-701.	2005	JEDEC	0
722	MO-257-B	Registration - Plastic Fine Pitch Quad No-Lead Staggered Two Row Thermally Enhanced Package Family. H(U,V,W)F-PQFN. Item 11.11-707.	2005	JEDEC	0
723	SO-004A	Registration - Connector Outline for DDR and DDR2 Micro DIMM Mezzanine, 214 pin, 0.4 mm Lead Centers. Item 11.14-076.	2005	JEDEC	0
724	SO-005A	Registration - 200 pin Mini DIMM with 0.60 mm Lead Centers Socket Outline	2005	JEDEC	0

725	TO-247-E_01	Registration - Flange-Mounted Header Family, Peripheral Leads. Item 11.10-425. This document contains editorial change made 11/05.	2005	JEDEC	0
726	SPP-017-C	Standard Practices and Procedures - Standard Overall Profile Height Codes for Packages. RESCINDED, March 2009	2004	JEDEC	0
727	MO-258-A	Registration - 200 pin DDR MiniDIMM. 0.60 mm Lead Centers. Item 11.14-069.	2004	JEDEC	0
728	MO-251-A	Registration - Thermally Enhanced Plastic Very Thick, Quad Flat No Lead Package. HE-PQFP-N. Item 11.11-657.	2004	JEDEC	0
729	MO-254-A	Registration - Thermally Enchanced Plastic Low and Thin Profile Fine Pitch Quad Flat No Lead Package. HLF-PQFPN, HTF-PQFPN. Item 11.11-686.	2004	JEDEC	0
730	MO-249-A	Registration - Thin Small Outline, Plastic Surface Mount Header, 8.89 mm Body Family. R-PDSO-G/TSOP11. Item 11.11-668.	2004	JEDEC	0
731	JESD82-1A	DEFINITION OF CVF857 PLL CLOCK DRIVER FOR REGISTERED PC1600, PC2100, PC2700, AND PC3200 DIMM APPLICATIONS:	2004	JEDEC	0
732	JESD90	A PROCEDURE FOR MEASURING P-CHANNEL MOSFET NEGATIVE BIAS TEMPERATURE INSTABILITIES	2004	JEDEC	0
733	JESD82-3B	DEFINITION OF THE SSTV16857 2.5 V, 14-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS:	2004	JEDEC	0
734	JESD82-6A	DEFINITION OF THE SSTV32852 2.5 V 24-BIT TO 48-BIT SSTL_2 REGISTERED BUFFER FOR 1U STACKED DDR DIMM APPLICATIONS:	2004	JEDEC	0
735	JESD82-7A	DEFINITION OF THE SSTU32864 1.8-V CONFIGURABLE REGISTERED BUFFER FOR DDR2 RDIMM APPLICATIONS:	2004	JEDEC	0
736	JESD82-8.01	STANDARD FOR DEFINITION OF CU877 PLL CLOCK DRIVE FOR REGISTERED DDR2 DIMM APPLICATION	2004	JEDEC	0
737	MO-211-C	Registration - Die Size Ball Grid Array, Fine Pitch, Thin/Very Thin/Extremely Thin Profile. X-DSBGA. Item 11.4-631.	2004	JEDEC	0
738	JEP84A	RECOMMENDED PRACTICE FOR MEASUREMENT OF TRANSISTOR LEAD TEMPERATURE:	2004	JEDEC	0
739	JS9702	IPC/JEDEC-9702: MONOTONIC BEND CHARACTERIZATION OF BOARD-LEVEL INTERCONNECTS (IPC/JEDEC-9702)	2004	JEDEC	0
740	JESD97	MARKING, SYMBOLS, AND LABELS FOR IDENTIFICATION OF LEAD (Pb) FREE ASSEMBLIES, COMPONENTS, AND DEVICES - SUPERSEDED BY J-STD-609, August 2007	2004	JEDEC	0
741	JEP149	APPLICATION THERMAL DERATING METHODOLOGIES:	2004	JEDEC	0
742	JEP137B	COMMON FLASH INTERFACE (CFI) IDENTIFICATION CODES:	2004	JEDEC	0
743	JESD75-4	BALL GRID ARRAY PINOUT FOR 1-, 2-, AND 3-BIT LOGIC FUNCTIONS:	2004	JEDEC	0
744	JESD75-5	SON/QFN PACKAGE PINOUTS STANDARDIZED FOR 1-, 2-, AND 3-BIT LOGIC FUNCTIONS	2004	JEDEC	0
745	JESD8-16A	BUS INTERCONNECT LOGIC (BIC) FOR 1.2 V	2004	JEDEC	0
746	JESD8-17	DRIVER SPECIFICATIONS FOR 1.8 V POWER SUPPLY POINT-TO-POINT DRIVERS	2004	JEDEC	0
747	JESD60A	A PROCEDURE FOR MEASURING P-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION AT MAXIMUM GATE CURRENT UNDER DC STRESS:	2004	JEDEC	0
748	JESD33B	STANDARD METHOD FOR MEASURING AND USING THE TEMPERATURE COEFFICIENT OF RESISTANCE TO DETERMINE THE TEMPERATURE OF A METALLIZATION LINE:	2004	JEDEC	0
749	JESD24-12	THERMAL IMPEDANCE MEASUREMENT FOR INSULATED GATE BIPOLAR TRANSISTORS - (Delta VCE(on) Method)	2004	JEDEC	0
750	DG-4.18A	Design Requirements - Wafer Level Ball Grid Arrays (WLBGA).	2004	JEDEC	0
751	DG-4.15B	Design Requirements - Thin Small Outline Package, TSOP - Type 2.	2004	JEDEC	0
752	DO-220-B	Registration - Small Outline Plastic Surface Mount. PSOF-2. Item 10-431.	2004	JEDEC	0
753	MODULE4.20.12	214-Pin DDR2 SDRAM Unbuffered MicroDIMM Design Specification	2004	JEDEC	0
754	MPDRAM3.10.3	Word Wide Graphics DRAM	2004	JEDEC	0
755	SDRAM3.11.2	Nibble Wide SDRAM	2004	JEDEC	0

756	SDRAM3.11.3	Byte Wide SDRAM	2004	JEDEC	0
757	JESD22-A105C	POWER AND TEMPERATURE CYCLING	2004	JEDEC	0
758	SPD4.1.2.4	SPD Annex D, DDR Synchronous DRAM (DDR SDRAM)	2004	JEDEC	0
759	MODULE4.20.8	184-Pin PC-2700 SDRAM Unbuffered DIMM - TSOP-Based DRAMs Design Specification	2004	JEDEC	0
760	MODULE4.20.9	100-Pin DDR SDRAM Unbuffered 32b-DIMM Design Specification	2004	JEDEC	0
761	MODULE4.20.5	184 Pin, PC-1600/PC-2100 DDR SDRAM Unbuffered DIMM Design Specification.	2003	JEDEC	0
762	MODULE4.20.6	200 Pin, PC-2700/PC-2100/PC-1600 Unbuffered SO-DIMM SDRAM Reference Design Specification	2003	JEDEC	0
763	MODULE4.20.2	168 Pin, PC-133 SDRAM Registered DIMM Design Specification	2003	JEDEC	0
764	MODULE4.20.3	144 Pin, PC133 SDRAM Unbuffered SO-DIMM, Reference Design Specification	2003	JEDEC	0
765	MODULE4.5.14	240-Pin Unbuffered and Registered DDR2 SDRAM DIMM Family	2003	JEDEC	0
766	MODULE4.5	4.5 Table of Contents - Eight Byte Modules	2003	JEDEC	0
767	MODULE4.5.10	184 Pin Unbuffered DDR SDRAM DIMM	2003	JEDEC	0
768	SPD4.1.2.5	SPD Annex E, SDRAM	2003	JEDEC	0
769	SDRAM3.11.5.2	DDR Specific SDRAM Functions	2003	JEDEC	0
770	SDRAM3.2	Device Specification Annex for JESD21-C	2003	JEDEC	0
771	SPD4.1.2.1	SPD Annex A, Table of Memory Types	2003	JEDEC	0
772	JESD22-B100B	PHYSICAL DIMENSION:	2003	JEDEC	0
773	SRAM3.7.5	Byte Wide SRAM	2003	JEDEC	0
774	DO-214-D	Registration - Power Plastic Outline, Surface Mount with 1-Lead C-Bend Terminal. Includes Errata to DO-214, May 1998. Item 11.1-654(e).	2003	JEDEC	0
775	DO-215-D	Registration - Small Outline Plastic Surface Mount Package with 2 Gullwing Terminals. Includes Errata to DO-215, May 1998. Item 11.1-655(e).	2003	JEDEC	0
776	CO-034-D	Registration - Addition of numerous N4 body sizes to variations AE and AF of Low Profile Matrix Tray for Handling and Shipping Thin Grid Array Devices Registration. Item 11.5-634.	2003	JEDEC	0
777	JESD65B	DEFINITION OF SKEW SPECIFICATIONS FOR STANDARD LOGIC DEVICES:	2003	JEDEC	0
778	JESD68.01	COMMON FLASH INTERFACE (CFI):	2003	JEDEC	0
779	JESD8-15A	STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL_18):	2003	JEDEC	0
780	JEP147	PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER (VNA):	2003	JEDEC	0
781	JEP145	GUIDELINE FOR ASSESSING THE CURRENT-CARRYING CAPABILITY OF THE LEADS IN A POWER PACKAGE SYSTEM:	2003	JEDEC	0
782	JEP119A	A PROCEDURE FOR EXECUTING SWEAT:	2003	JEDEC	0
783	JEP104C.01	REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES:	2003	JEDEC	0
784	MO-216-E	Registration - Thin Profile, Square and Rectangular, Ball Grid Array (BGA) Family, for 1.00 mm and 0.80 mm Pitch. T-XBGA, TF-XBGA, TR-XBGA. Item 11.11-658.	2003	JEDEC	0
785	MO-192-F	Registration - Low Profile Square Ball Grid Array Family. S-LBGA-B/LBGA.	2003	JEDEC	0
786	MO-149-F	Registration - Tape Ball Grid Array. XBGA-B/TBGA. Item 11.4-665.	2003	JEDEC	0

787	JESD82-4B	STANDARD FOR DEFINITION OF THE SSTV16859 2.5 V, 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR STACKED DDR DIMM APPLICATIONS:	2003	JEDEC	0
788	JESD91A	METHOD FOR DEVELOPING ACCELERATION MODELS FOR ELECTRONIC COMPONENT FAILURE MECHANISMS	2003	JEDEC	0
789	JESD92	PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS:	2003	JEDEC	0
790	MO-250-A	Registration - New family of Thermally Enhanced Plastic Very Thin and Very Very Thin Pitch Bumped Quad Flat No Lead Packages. HP-VFQFP-NB, HP-WFQFP-NB. Item 11.11-679.	2003	JEDEC	0
791	MO-243-A	Registration - Thermally Enhanced Plastic Very Thin and Very Very Thin Fine Pitch Bumped Quad Flat No Lead Package. HP-VFQFP-NB & HP-WFQFP-NB.	2003	JEDEC	0
792	MO-245-A	Registration - High Profile Plastic Thermally Enhanced Enlarged Pitched Dual Flat No Lead Package. HE-PDFP-N. Item 11.11-638.	2003	JEDEC	0
793	MO-238-A	Registration - Stacked TSOP II Package Family (2 High). R-PDSO-G. Item 11.11-635	2003	JEDEC	0
794	MO-241-B	Registration - Dual in-line compatible, thermally enhanced, plastic very thin fine pitch, QFN package family, includes addition of Very Thin Profile variations. HW-PQFP-N/HV-PQFP-N/PSO-N. Item 11.11-662.	2003	JEDEC	0
795	MO-233-C	Registration - Mixed Pitch (0.80 & 1.00 mm), Rectangular Die Size, Fine Dual Pitch Ball Grid Array (DSBGA) family. TFR-XBGA-N. Item 11.4-611	2003	JEDEC	0
796	MO-235-B	Registration - Plastic peripheral leaded, flange mounted package family with revision of lead dimensions (5 lead). R-PSFM-G. Item 11.10-423.	2003	JEDEC	0
797	SO-001B	Registration - 240 pin DDR2 SDRAM, 1.00 mm contact centers, Socket Outline. Item 11.14-061.	2003	JEDEC	0
798	SO-002B	Registration - 244 Pin DDR2/DDR3 Mini DIMM with 0.60 mm Lead Centers Socket Outline. Item 11.14-122.	2003	JEDEC	0
799	SPP-020A	WITHDRAWN: Standard Practices and Procedures - Rectangular Grid Array Terminal Position Numbering. Item 11.2-641(S)	2003	JEDEC	0
800	TO-273-B	Registration - Plastic Flange Mounted Package, 3 Leads (IR's Modification of 3 Lead TO-220). Item 11.10-389. Addition of patent note in drawing. R-PSIP-F3. Item 11.1-664(e), .	2003	JEDEC	0
801	TO-059	Reinstated.	2003	JEDEC	0
802	TO-220-K	Registration - General update and INACTIVATION of variation AA to flange mounted header family (peripheral terminals). Items 11.10-421.	2002	JEDEC	0
803	TO-251-D	Registration - The general update and change of lead dimensions for flange mounted family, insertion mount (peripheral terminals). R-PSIP-F3. Item 11.10-417	2002	JEDEC	0
804	TO-261-C	Registration - Dimensional update and removal of land pattern from the SOP/SOT registration. R-PDSO-G. Item 11.10-416	2002	JEDEC	0
805	MO-239-B	Registration - Thermally Enhanced Plastic Very Thin Dual Row Fine Pitch Quad Flat No Lead Package. HP-VFQFP-N. Item 11.11-680	2002	JEDEC	0
806	JESD82-5	STANDARD FOR DESCRIPTION OF A 3.3 V, ZERO DELAY CLOCK DISTRIBUTION DEVICE COMPLIANT WITH THE JESD21-C PC133 REGISTERED DIMM SPECIFICATION	2002	JEDEC	0
807	JESD8-9B	ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2): Includes Errata and Corrected Page 7 as of October 18, 2002.	2002	JEDEC	0
808	MO-220-D	Registration - Consolidation and addition of numerous variations to the thermally enhanced plastic very thin fine pitch quad flat, no lead package. HP-VFQFP-N/HP-WFQFP-N. Item 11.11-620.	2002	JEDEC	0
809	MO-214-B	Registration - Addition of 172 pin Micro DIMM variations and modification of terminal postional tolerance to Micro DIMM registration. Item 11.14-049.	2002	JEDEC	0
810	MO-158-D	Registration - The addition of 47.5, 50.0, 52.5 and 55.0 mm body variations with 1.27 mm and 1.00 mm ball pitch to Column Grid Array Registration. Item 11.10-415. CBGA-X/CCBA	2002	JEDEC	0
811	MO-161-F	Registration - 168 pin DIMM. Multiple Keyway Dual-In-Line Memory Module (DIMM), 1.27 mm contact centers. Addition of the 100 pin variation GA-XX and the INACTIVATION of the 168 pin right polarized configuration to DIMM registration. Item 11.14-055/056.	2002	JEDEC	0
812	JEP140	BEADED THERMOCOUPLE TEMPERATURE MEASUREMENT OF SEMICONDUCTOR PACKAGES	2002	JEDEC	0

813	JEP142	GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID/MCM PRODUCTS:	2002	JEDEC	0
814	JESD282B.01	SILICON RECTIFIER DIODES:	2002	JEDEC	0
815	JESD62-A	OUTLIER IDENTIFICATION AND MANAGEMENT SYSTEM FOR ELECTRONIC COMPONENTS, RESCINDED January 2009. Replaced by JESD50.	2002	JEDEC	0
816	DG-4.10D	Design Requirements - Generic Matrix Tray for Handling and Shipping, includes addition of optional side-wall bar code feature.	2002	JEDEC	0
817	CO-029-H	Registration - Thin Matrix Tray for Shipping and Handling of Ball Grid Packages. Includes Change to Note 18. Item 11.5-633	2002	JEDEC	0
818	SDRAM3.11.5.1	General SDRAM Functions	2002	JEDEC	0
819	MODULE4.20.4	PC-1600/PC-2100 DDR SDRAM Registered DIMM Design Specification (184 Pin)	2002	JEDEC	0
820	MODULE4.20.1	Standard Template for JEDEC Module Standards	2001	JEDEC	0
821	MODULE4.5.7	168 Pin Registered SDRAM DIMM Family	2001	JEDEC	0
822	MODULE4.5.2	200 Pin SDRAM DIMM	2001	JEDEC	0
823	SPD4.1.2.2	SPD Annex B, Table of Superset Memory Types	2001	JEDEC	0
824	MODULE4	Module Introduction	2001	JEDEC	0
825	SRAM3.7	SRAM Introduction	2001	JEDEC	0
826	JESD51-11	TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE THERMAL MEASUREMENT:	2001	JEDEC	0
827	JESD35-A	PROCEDURE FOR WAFER-LEVEL-TESTING OF THIN DIELECTRICS:	2001	JEDEC	0
828	JESD28-1	N-CHANNEL MOSFET HOT CARRIER DATA ANALYSIS:	2001	JEDEC	0
829	JESD28-A	A PROCEDURE FOR MEASURING N-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION UNDER DC STRESS:	2001	JEDEC	0
830	JESD8-13	SCALABLE LOW-VOLTAGE SIGNALING FOR 400 MV (SLVS-400):	2001	JEDEC	0
831	JESD75-1	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16, 18, AND 20-BIT LOGIC FUNCTIONS USING A 54 BALL PACKAGE:	2001	JEDEC	0
832	JESD75-2	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16-BIT LOGIC FUNCTIONS:	2001	JEDEC	0
833	JESD75-3	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 8-BIT LOGIC FUNCTIONS:	2001	JEDEC	0
834	JESD76-1	STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (WIDE RANGE OPERATION):	2001	JEDEC	0
835	JESD76-2	STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (NORMAL RANGE OPERATION):	2001	JEDEC	0
836	JESD76-3	STANDARD DESCRIPTION OF 1.5 V CMOS LOGIC DEVICES:	2001	JEDEC	0
837	JESD72	TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS:	2001	JEDEC	0
838	JESD73-1	STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES:	2001	JEDEC	0
839	JESD73-2	STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES WITH INTEGRATED CHARGE PUMPS:	2001	JEDEC	0
840	JESD73-3	STANDARD FOR DESCRIPTION OF 3867 - 2.5 V, SINGLE 10-BIT, 2-PORT, DDR FET SWITCH:	2001	JEDEC	0
841	JESD73-4	STANDARD FOR DESCRIPTION OF 3877 - 2.5 V, DUAL 5-BIT, 2-PORT, DDR FET SWITCH:	2001	JEDEC	0
842	MO-190-D	Registration - 144 Pin Small Outline Dual-In-Line Memory Module (DIMM) Family 0.8 mm Lead Centers with addition of optional beveled edge to SODIMM Family. Item 11.14-048.	2001	JEDEC	0
843	MO-153-F	Registration - Plastic Thin SSOP R-PDSO-G/TSSOP/HTSSOF, Addition of A1 clarification note (note 14). Item 11.11-603	2001	JEDEC	0
844	MO-180-B	Registration - Plastic SOP, 13.30 mm Wide Body, 1.27 mm Pitch, with addition of a 90 lead Small Outline Package as variation CA. Item 11.11-571.	2001	JEDEC	0
845	MO-208-C	Registration - Plastic Thin Fine Pitch Quad Flat, No Lead, Package. Registration of Quad, Single and Double Row SON Packages. The addition of 7 new thermal variations. Item 11.11-599.	2001	JEDEC	0

846	MO-204-B	Registration - Plastic Quad Flatpack (PQFP) Outline with Exposed Heat Sink. Thermally Enhanced PQFPs. Addition of standard height, variations BA, BB, BC, BD, and BE with Exposed Heat Sink.	2001	JEDEC	0
847	MO-217-B	Registration - Very Very Thin Quad Bottom Terminal Chip Carrier Family with Addition of variations AE, AF, AG, BE, BF, and BG. W-PBCC-B/WH-PBCC-B. Item 11.11-621.	2001	JEDEC	0
848	MO-228-A	Registration - Square, Dual Pitch, FBGA Family. Item 11.11-581.	2001	JEDEC	0
849	MO-226-B	Registration - Change the A4 dimension and value in the Plastic Small Outline Heatslug Package , 7.50 mm Body Wide, 1.0 mm Lead Pitch (H-PDSO-G). Item 11.11-589.	2001	JEDEC	0
850	MO-221-C	Registration - Extremely Thin, Two Row Cavity Down, 0.50 mm Pitch BGA Family. The addition of -2, max matrix, variations to XFBGA. Item 11.11-604.	2001	JEDEC	0
851	JESD82-2	STANDARD FOR DESCRIPTION OF A 3.3 V, 18-BIT, LVTTL I/O REGISTER FOR PC133 REGISTERED DIMM APPLICATIONS:	2001	JEDEC	0
852	JESD87	STANDARD TEST STRUCTURE FOR RELIABILITY ASSESSMENT OF AlCu METALLIZATIONS WITH BARRIER MATERIALS	2001	JEDEC	0
853	JESD85	METHODS FOR CALCULATING FAILURE RATES IN UNITS OF FITS	2001	JEDEC	0
854	MO-230-A	Registration - Plastic Small Outline Package with Exposed Heat Sink.	2001	JEDEC	0
855	MO-231-A	REGISTRATION - Thermally enhanced single in-line surface mount package. 21.50 mm Body Width, 1.40 mm Lead Pitch. R-PSIP-Fxx. Item 11.11-590.	2001	JEDEC	0
856	MO-232-A	Registration - Thermally Enhanced Low Profile Plastic Dual, Flat No Lead Package. L-PDFP-N. Item 11.10-412	2001	JEDEC	0
857	SPP-019-A	Standard Practices and Procedures - New SPP to clarify how A1 is to be measured. Item 11.2-595s	2001	JEDEC	0
858	MS-026-D	Standard - Low/Thin Profile Plastic Quad Flat Package, 2.00 mm Footprint, Optional Heat. Item 11.11-521S.	2001	JEDEC	0
859	TO-276-A	Registration - Bottom Terminal Ceramic Chip Carrier Family. Item 11.10-408.	2001	JEDEC	0
860	TO-275-A	Registration - Plastic Flange Mounted, 2 Lead, Power Package. Item 11.10-405	2000	JEDEC	0
861	MO-133-A	Replaced - See MS-024-E.	2000	JEDEC	0
862	JESD82	DEFINITION OF CDCV857 PLL CLOCK DRIVER FOR REGISTERED DDR DIMM APPLICATIONS:	2000	JEDEC	0
863	MO-227-A	Registration - 232 Pin DDR SDRAM DIMM Family, 1.00 mm Pitch. Item 11.14-042	2000	JEDEC	0
864	MO-215-A	Registration - 210 Pin SDRAM Dual-In-Line Memory Module (DIMM) Family, 1.00 mm Contact Centers. Item 11.14-039. This Outline is Now Inactive. Item 11.14-047.	2000	JEDEC	0
865	MO-169-B	Registration - Addition of variations, BA, BB, BC, and BD, to Plastic, Surface Mounted Header Family. Item 11.10-406	2000	JEDEC	0
866	JESD64-A	STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES WITH 3.6 V CMOS TOLERANT INPUTS AND OUTPUTS:	2000	JEDEC	0
867	JESD51- 9	TEST BOARDS FOR AREA ARRAY SURFACE MOUNT PACKAGE THERMAL MEASUREMENTS:	2000	JEDEC	0
868	JESD76	DESCRIPTION OF 1.8 V CMOS LOGIC DEVICES:	2000	JEDEC	0
869	JESD286-B	STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES:	2000	JEDEC	0
870	JESD51-10	TEST BOARDS FOR THROUGH-HOLE PERIMETER LEADED PACKAGE THERMAL MEASUREMENTS:	2000	JEDEC	0
871	JEP139	GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING:	2000	JEDEC	0
872	JEP120A	INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS:	2000	JEDEC	0
873	DRAM3.9.4	Word Wide DRAM	2000	JEDEC	0
874	DRAM3.9.5	DRAM Operational Features	2000	JEDEC	0
875	MODULE4.5.11	184 Pin Unbuffered SDR SDRAM DIMM Family	2000	JEDEC	0
876	MODULE4.5.12	184 Pin DIMM Family Supplementary Design Standards	2000	JEDEC	0
877	MODULE4.5.13	144 Pin and 168 Pin PEMM Families with EDO-DRAM and SDRAM	2000	JEDEC	0

878	MODULE4.5.8	144 Pin SGRAM/SDRAM SO-DIMM Family	2000	JEDEC	0
879	DG-4.9A	Design Requirements - Generic Matrix Tray for Handling and Shipping (Low Stacking Profile for BGA Packages).	2000	JEDEC	0
880	DG-4.4A	Design Requirements - Quad Flatpack	2000	JEDEC	0
881	MODULE4.5.9	144 Pin DDR SGRAM SO-DIMM	1999	JEDEC	0
882	MODULE4.5.1	168 Pin DRAM DIMM	1999	JEDEC	0
883	MODULE4.5.3	168 Pin Unbuffered DRAM DIMM	1999	JEDEC	0
884	MODULE4.5.4	168 Pin Unbuffered SDRAM DIMM	1999	JEDEC	0
885	MODULE4.5.5	144 Pin DRAM SO-DIMM	1999	JEDEC	0
886	MODULE4.5.6	144 Pin SDRAM SO-DIMM	1999	JEDEC	0
887	SDRAM3.11.5.3	Enhanced SDRAM (ESDRAM) Specific SDRAM Functions	1999	JEDEC	0
888	SDRAM3.11.5.4	VCSDRAM Specific SDRAM Functions	1999	JEDEC	0
889	SDRAM3.11.6	SDRAM Parametric Standards	1999	JEDEC	0
890	SPD4.1.2.8	SPD Annex H, ESDRAM Superset	1999	JEDEC	0
891	DRAM3.9.1	Bit Wide DRAM	1999	JEDEC	0
892	DRAM3.9.2	Nibble Wide DRAM	1999	JEDEC	0
893	DRAM3.9.3	Byte Wide DRAM	1999	JEDEC	0
894	EPROM3.4.2	Word Wide EPROM	1999	JEDEC	0
895	JEP113B	SYMBOL AND LABELS FOR MOISTURE-SENSITIVE DEVICES	1999	JEDEC	0
896	JEP136	SIGNATURE ANALYSIS:	1999	JEDEC	0
897	JEP138	USER GUIDELINES FOR IR THERMAL IMAGING DETERMINATION OF DIE TEMPERATURE:	1999	JEDEC	0
898	JESD75	BALL GRID ARRAY PINOUTS STANDARDIZED FOR 32-BIT LOGIC FUNCTIONS:	1999	JEDEC	0
899	JESD70	2.5 V BiCMOS LOGIC DEVICE FAMILY SPECIFICATION WITH 5 V TOLERANT INPUTS AND OUTPUTS:	1999	JEDEC	0
900	JESD71	STANDARD TEST AND PROGRAMMING LANGUAGE (STAPL):	1999	JEDEC	0
901	JESD51- 6	INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR):	1999	JEDEC	0
902	JESD51- 7	HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES:	1999	JEDEC	0
903	JESD51- 8	INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - JUNCTION-TO-BOARD:	1999	JEDEC	0
904	JESD51- 5	EXTENSION OF THERMAL TEST BOARD STANDARDS FOR PACKAGES WITH DIRECT THERMAL ATTACHMENT MECHANISMS:	1999	JEDEC	0
905	JESD73	DESCRIPTION OF 5 V BUS SWITCH WITH TTL-COMPATIBLE CONTROL INPUTS:	1999	JEDEC	0
906	JESD66	TRANSIENT VOLTAGE SUPPRESSOR STANDARD FOR THYRISTOR SURGE PROTECTIVE DEVICE:	1999	JEDEC	0
907	JESD67	I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND RECEIVER THRESHOLD:	1999	JEDEC	0
908	MO-177-A	Registration - Rescission of 200 Pin Small Outline Dual-In-Line Memory Module (DIMM) Family, 0.65 mm Pitch. Item 11.14-044.	1999	JEDEC	0
909	J-STD-035	JOINT IPC/JEDEC STANDARD FOR ACOUSTIC MICROSCOPY FOR NONHERMETRIC ENCAPSULATED ELECTRONIC COMPONENTS	1999	JEDEC	0
910	JESD80	STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES:	1999	JEDEC	0
911	JESD63	STANDARD METHOD FOR CALCULATING THE ELECTROMIGRATION MODEL PARAMETERS FOR CURRENT DENSITY AND TEMPERATURE:	1998	JEDEC	0
912	JEP134	GUIDELINES FOR PREPARING CUSTOMER-SUPPLIED BACKGROUND INFORMATION RELATING TO A SEMICONDUCTOR-DEVICE FAILURE ANALYSIS:	1998	JEDEC	0

913	JEP132	PROCESS CHARACTERIZATION GUIDELINE:	1998	JEDEC	0
914	SPD4.1.2.6	SPD Annex F, Address Multiplexed ROM	1998	JEDEC	0
915	SPD4.1.2.3	SPD Annex C, Fast Page and Extended Data Out RAM	1998	JEDEC	0
916	DG-4.16A	Design Requirements - Plastic Ultra-Thin Small outline No-Lead Package. R-PDSO-N/USON.	1998	JEDEC	0
917	CS-005-B	Standard - TSOP II, Thin Matrix Tray for Shipping and Handling of FBGA's. Item 11.5-519.	1998	JEDEC	0
918	CO-033-A	Registration - Plastic Chip Carrier (PLCC) Shipping/Handling Tubes. Item 11.5-501.	1998	JEDEC	0
919	SPD4.1.1	Memory Module Nomenclature	1997	JEDEC	0
920	SDRAM3.11.1	Bit Wide SDRAM	1997	JEDEC	0
921	MODULE4.2	One Byte Modules	1997	JEDEC	0
922	MODULE4.3	Two Byte Modules Cards	1997	JEDEC	0
923	MODULE4.4.1	64 & 72 Pin ZIP/SIMM SRAM Module	1997	JEDEC	0
924	MODULE4.4.2	72 Pin DRAM SIMM	1997	JEDEC	0
925	MODULE4.4.3	88 Pin DRAM Card	1997	JEDEC	0
926	MODULE4.4.4	72 Pin DRAM SO-DIMM	1997	JEDEC	0
927	MODULE4.4.5	88 Pin DRAM SO-DIMM	1997	JEDEC	0
928	MODULE4.4.6	112 Pin MPDRAM DIMM	1997	JEDEC	0
929	MODULE4.4.7	80 Pin EEPROM SIMM	1997	JEDEC	0
930	MODULE4.4.8	100 Pin DRAM, SDRAM, and ROM DIMM	1997	JEDEC	0
931	MODULE4.4.TOC	Four Byte Modules and Cards Table of Contents	1997	JEDEC	0
932	MODULE4.6.1	278 Pin Buffered SDRAM DIMM	1997	JEDEC	0
933	MODULE4.6	4.6 Table of Contents - Sixteen Byte Modules	1997	JEDEC	0
934	EEPROM3.5	EEPROM Introduction	1997	JEDEC	0
935	EPROM3.4	EPROM Introduction	1997	JEDEC	0
936	EPROM3.4.1	Byte Wide	1997	JEDEC	0
937	SRAM3.7.6	Byte Wide ECL SRAM	1997	JEDEC	0
938	SRAM3.7.2	Bit Wide ECL SRAM	1997	JEDEC	0
939	DRAM3.9.TOC	Dynamic Random Access Memory (DRAM) Table of Contents	1997	JEDEC	0
940	MPDRAM3.10.1	Nibble Wide MPDRAM	1997	JEDEC	0
941	MPDRAM3.10.2	Byte Wide MPDRAM	1997	JEDEC	0
942	MPDRAM3.10.4	MPDRAM Optional Features	1997	JEDEC	0
943	JESD39-A	QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997.	1997	JEDEC	0
944	JESD59	BOND WIRE MODELING STANDARD:	1997	JEDEC	0
945	JEP129	THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP)- SUPERSEDED BY JESD51-4, September 1997.	1997	JEDEC	0
946	MO-201-A	Registration - Stacked TSOPII Package (2 and 4 High). Item 11.11-429.	1997	JEDEC	0
947	JESD8-8	ADDENDUM No. 8 to JESD8 - STUB SERIES TERMINATED LOGIC FOR 3.3 VOLTS (SSTL_3) A 3.3 V VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS	1996	JEDEC	0
948	JESD53	MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: RESCINDED, October 2002	1996	JEDEC	0
949	JESD51- 3	LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES:	1996	JEDEC	0

950	JESD36	STANDARD DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE, 5 V TOLERANT CMOS LOGIC DEVICES:	1996	JEDEC	0
951	JESD35-2	ADDENDUM No. 2 to JESD35 - TEST CRITERIA FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS:	1996	JEDEC	0
952	JESD32	STANDARD FOR CHAIN DESCRIPTION FILE:	1996	JEDEC	0
953	JESD24-11	ADDENDUM No. 11 to JESD24 - POWER MOSFET EQUIVALENT SERIES GATE RESISTANCE TEST METHOD:	1996	JEDEC	0
954	JESD57	TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION:	1996	JEDEC	0
955	JESD54	STANDARD FOR DESCRIPTION OF 54/74ABTXXX AND 74BCXXX TTL-COMPATIBLE BiCMOS LOGIC DEVICES:	1996	JEDEC	0
956	JESD55	STANDARD FOR DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE BiCMOS LOGIC DEVICES:	1996	JEDEC	0
957	JESD43	COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS - SUPERSEDED BY EIA-671, November 1996.	1996	JEDEC	0
958	JESD29-A	FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996.	1996	JEDEC	0
959	JEP103A	SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS	1996	JEDEC	0
960	JEP126	GUIDELINE FOR DEVELOPING AND DOCUMENTING PACKAGE ELECTRICAL MODELS DERIVED FROM COMPUTATIONAL ANALYSIS:	1996	JEDEC	0
961	JEP128	GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER LEVEL ELECTRICAL TESTING:	1996	JEDEC	0
962	CS-008-A	Standard - TSOP-I, Thin Matrix Tray for Shipping and Handling. Item 11.4-437S.	1996	JEDEC	0
963	DG-4.13	Design Requirements - Metric Small Outline J-Leaded Package Design Guide	1996	JEDEC	0
964	CO-032-A	Registration - Thin Matrix Tray for Handling and Shipping Small Outline J- Lead Packages (SOJ). Item 11.5-446.	1996	JEDEC	0
965	CS-004-B	Standard - Thin Matrix Tray for MQFP Shipping. Item 11.5-436S	1996	JEDEC	0
966	CO-030-A	Registration - Thin Matrix Mini Tray for Shipping and Handling. Item 11.5-427.	1995	JEDEC	0
967	CO-031-A	Registration - Thick Matrix Mini Tray For Shipping and Handling. Item 11.5-426.	1995	JEDEC	0
968	SRAM3.7.3	Nibble Wide SRAM	1995	JEDEC	0
969	SRAM3.7.1	Bit Wide TTL SRAM	1995	JEDEC	0
970	JEP123	GUIDELINE FOR MEASUREMENT OF ELECTRONIC PACKAGE INDUCTANCE AND CAPACITANCE MODEL PARAMETERS:	1995	JEDEC	0
971	JESD16-A	ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM)	1995	JEDEC	0
972	JESD51	METHODOLOGY FOR THE THERMAL MEASUREMENT OF COMPONENT PACKAGES (SINGLE SEMICONDUCTOR DEVICE)	1995	JEDEC	0
973	JESD52	STANDARD FOR DESCRIPTION OF LOW VOLTAGE TTL-COMPATIBLE CMOS LOGIC DEVICES:	1995	JEDEC	0
974	JESD38	STANDARD FOR FAILURE ANALYSIS REPORT FORMAT:	1995	JEDEC	0
975	JESD35-1	ADDENDUM No. 1 to JESD35 - GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS:	1995	JEDEC	0
976	JESD51- 1	INTEGRATED CIRCUIT THERMAL MEASUREMENT METHOD - ELECTRICAL TEST METHOD (SINGLE SEMICONDUCTOR DEVICE):	1995	JEDEC	0
977	JEP101-C	JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS: RESCINDED, May 2006	1995	JEDEC	0
978	JEP109-C	GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:	1995	JEDEC	0
979	JESD41	REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: RESCINDED June 2002.	1995	JEDEC	0
980	JESD8-6	ADDENDUM No. 6 to JESD8 - HIGH SPEED TRANSCEIVER LOGIC (HSTL)- A 1.5 V OUTPUT BUFFER SUPPLY VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:	1995	JEDEC	0
981	JESD22-A112-A	MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999.	1995	JEDEC	0
982	JEP124	GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999.	1995	JEDEC	0

983	MO-150-B	Registration - Plastic Shrink Small Outline Package (SSOP), 5.3 mm Body Width. R-PDSO-G.	1994	JEDEC	0
984	MO-147-A	Registration - Small Outline J-Lead (SOJ) Ceramic Chip Carrier, .415 inch Body, .050 inch Lead Spacing. R-CDSO-J.	1994	JEDEC	0
985	JESD8-1	ADDENDUM No. 1 to JESD8: INTERFACE STANDARD FOR LOW VOLTAGE TTL-COMPATIBLE (LVTTL) VLSI DIGITAL CIRCUITS	1994	JEDEC	0
986	EIA623	PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS	1994	JEDEC	0
987	SPP-014	Standard Practices and Procedures - Mold Flash, Interlead Flash, Gate Burrs and Protrusion for Plastic Packages. Item 11.2-379.	1994	JEDEC	0
988	JEP117	GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997.	1994	JEDEC	0
989	JESD3-C	STANDARD DATA TRANSFER FORMAT BETWEEN DATA PREPARATION SYSTEM AND PROGRAMMABLE LOGIC DEVICE PROGRAMMER:	1994	JEDEC	0
990	JESD24-10	ADDENDUM No. 10 to JESD24 - TEST METHOD FOR MEASUREMENT OF REVERSE RECOVERY TIME trr FOR POWER MOSFET DRAIN-SOURCE DIODES:	1994	JEDEC	0
991	JESD40	PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994	1994	JEDEC	0
992	SRAM3.7.4	Nibble Wide ECL SRAM	1994	JEDEC	0
993	SDRAM3.11	Synchronous Dynamic Random Access Memory (SDRAM)	1994	JEDEC	0
994	CO-010-E	Registration - Tray for Handling and Shipping of PGA Packages. Item 11.5-382	1994	JEDEC	0
995	CO-013-B	Registration - Generic Carrier Family. Variations AA-AC. Item 11.5-314.	1993	JEDEC	0
996	CO-015-B	Registration - Tray for Handling and Shipping of PQFP Packages, 52, 68, 84, 100, 132, 164, 196 and 244 Pins. Variations AA-AG. Item 11.5-249	1993	JEDEC	0
997	CS-002-A	Standard - Thin Matrix Tray for Handling and Shipping of Plastic Qual Flatpack Packages (PQFP). Variations AA-AG. Item 11.5-311.	1993	JEDEC	0
998	CS-003-B	Standard - Thin Matrix Tray for Handling and Shipping PLCC Packages. Variations AA-AL. Item 11.5-312.	1993	JEDEC	0
999	PROM3.3.1	Nibble Wide PROM	1993	JEDEC	0
1000	PROM3.3.2	Byte Wide PROM	1993	JEDEC	0
1001	PROM3.3.3-4	Word Wide PROM, DIP to SO Conversion	1993	JEDEC	0
1002	GS-003C	STANDARD - Dual In-Line Gauge. (Ties with all Shrink P-DIPs). Variations AA-BD. Item 11.11-315.	1993	JEDEC	0
1003	JEP118	GUIDELINES FOR GaAs MMIC AND FET LIFE TESTING:	1993	JEDEC	0
1004	JESD18-A	STANDARD FOR DESCRIPTION OF FAST CMOS TTL COMPATIBLE LOGIC:	1993	JEDEC	0
1005	JESD12-1B	ADDENDUM No. 1 to JESD12 - TERMS AND DEFINITIONS FOR GATE ARRAYS AND CELL-BASED INTEGRATED CIRCUITS:	1993	JEDEC	0
1006	JESD27	CERAMIC PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES	1993	JEDEC	0
1007	JESD34	FAILURE-MECHANISM-DRIVEN RELIABILITY QUALIFICATION OF SILICON DEVICES:	1993	JEDEC	0
1008	JESD8-4	ADDENDUM No. 4 to JESD8 - CENTER-TAP-TERMINATED (CTT) INTERFACE LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:	1993	JEDEC	0
1009	JESD8-2	ADDENDUM No. 2 to JESD8 - STANDARD FOR OPERATING VOLTAGES AND INTERFACE LEVELS FOR LOW VOLTAGE EMITTER-COUPLED LOGIC (ECL) INTEGRATED CIRCUITS:	1993	JEDEC	0
1010	MO-148-A	Registration - Multichip Module (MCM) Ceramic Quad Flatpack Family. S-CQFP.	1993	JEDEC	0
1011	MO-138-A	Registration - 16 Lead Flange-Mounted Ceramic Power Package (Type 1). R-CDFM-T16.	1993	JEDEC	0
1012	MO-134-A	Registration - Ceramic Quad Flatpack Family (CQFP), 0.50 mm Lead Pitch with Ceramic Nonconductive Tie Bar. Item 11.10-317.	1992	JEDEC	0
1013	JES2	TRANSISTOR, GALLIUM ARSENIDE POWER FET, GENERIC SPECIFICATION:	1992	JEDEC	0
1014	JESD24- 8	ADDENDUM No. 8 to JESD24 - METHOD FOR REPETITIVE INDUCTIVE LOAD AVALANCHE SWITCHING:	1992	JEDEC	0
1015	JESD24- 9	ADDENDUM No. 9 to JESD24 - SHORT CIRCUIT WITHSTAND TIME TEST METHOD:	1992	JEDEC	0

1016	JESD320-A	CONDITIONS FOR MEASUREMENT OF DIODE STATIC PARAMETERS:	1992	JEDEC	0
1017	JESD37	STANDARD LOGNORMAL ANALYSIS OF UNCENSORED DATA, AND OF SINGLY RIGHT -CENSORED DATA UTILIZING THE PERSSON AND ROOTZEN METHOD:	1992	JEDEC	0
1018	ROM3.2.1	Byte Wide ROM	1992	JEDEC	0
1019	ROM3.2.2	Word Wide ROM	1992	JEDEC	0
1020	CO-019-A	Registration - TapePak Magazine Family, Metal, Coinstack. Variations AA-AC.	1992	JEDEC	0
1021	CO-012-C	Registration - Tray for Handling and Shipping of Metric Quad Flatpack (QFP) Packages. Variations AA-AE. Item 11.5-298/336.	1992	JEDEC	0
1022	CO-016-B	Registration - PLCC Tray for Handling and Shipping. Variations AA-AL. Item 11.5-281.	1991	JEDEC	0
1023	NVRAM3.6	NVRAM, Nonvolatile RAM	1991	JEDEC	0
1024	JESD24- 6	ADDENDUM No. 6 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR INSULATED GATE BIPOLAR TRANSISTORS:	1991	JEDEC	0
1025	JESD24- 2	ADDENDUM No. 2 to JESD24 - GATE CHARGE TEST METHOD:	1991	JEDEC	0
1026	JEP108-B	DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC -DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994.	1991	JEDEC	0
1027	JESD12-6	ADDENDUM No. 6 to JESD12 - INTERFACE STANDARD FOR SEMICUSTOM INTEGRATED CIRCUITS:	1991	JEDEC	0
1028	JEP116	CMOS SEMICUSTOM DESIGN GUIDELINES:	1991	JEDEC	0
1029	MO-026-D	Registration - Dual-In-Line (DIP) Family Plastic Shrink Package, .400 inch Row Spacing, .070 inch Pitch, 30, 32 and 36 Leads. Item 11.11-274.	1991	JEDEC	0
1030	JESD22-C100-A	HIGH TEMPERATURE CONTINUITY	1990	JEDEC	0
1031	JESD26-A	GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001	1990	JEDEC	0
1032	JESD20	STANDARD FOR DESCRIPTION OF 54/74ACXXXXX AND 54/74ACTXXXXX ADVANCED HIGH-SPEED CMOS DEVICES:	1990	JEDEC	0
1033	JESD20	STANDARD FOR DESCRIPTION OF 54/74ACXXXXX AND 54/74ACTXXXXX ADVANCED HIGH-SPEED CMOS DEVICES:	1990	JEDEC	0
1034	JESD24- 3	ADDENDUM No. 3 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFETS (DELTA SOURCE-DRAIN VOLTAGE METHOD):	1990	JEDEC	0
1035	JESD24- 4	ADDENDUM No. 4 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR BIPOLAR TRANSISTORS (DELTA BASE-EMITTER VOLTAGE METHOD):	1990	JEDEC	0
1036	JESD24- 5	ADDENDUM No. 5 to JESD24 - SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD:	1990	JEDEC	0
1037	CO-011-B	Registration - Ceramic Quad Flatpack Package (CQFP) Tray for Handling and Shipping. Item 11.5-259.	1990	JEDEC	0
1038	CO-009-A	Registration - Tape Automated Bonding (TAB) Tape Carrier Family, 35, 48, 70 mm. Variations AA-AD, BA-BB, CA-CD.	1989	JEDEC	0
1039	CO-014-A	Registration - 2 inch Leaded Quadpack Carrier.	1989	JEDEC	0
1040	JESD24- 1	ADDENDUM No. 1 to JESD24 - METHOD FOR MEASUREMENT OF POWER DEVICE TURN-OFF SWITCHING LOSS:	1989	JEDEC	0
1041	JEP115	POWER MOSFET ELECTRICAL DOSE RATE TEST METHOD:	1989	JEDEC	0
1042	JEP110	GUIDELINES FOR THE MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETS:	1988	JEDEC	0
1043	JESD12-5	ADDENDUM No. 5 to JESD12 - DESIGN FOR TESTABILITY GUIDELINES:	1988	JEDEC	0
1044	JESD17	LATCH-UP IN CMOS INTEGRATED CIRCUITS - SUPERSEDED BY JESD78, February 1999	1988	JEDEC	0
1045	CO-008-A	Registration - Fine Pitch Plastic Shipping Tube Family. Item 11.5-233	1988	JEDEC	0
1046	JESD19	GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A	1988	JEDEC	0
1047	CO-007-A	Registration - Pin Grid Array Package D132 Carrier Family. 0.100 inch Centers.	1987	JEDEC	0

1048	JESD321-C	NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES:	1987	JEDEC	0
1049	JESD12-4	ADDENDUM No. 4 to JESD12 - METHOD OF SPECIFICATION OF PERFORMANCE PARAMETERS FOR CMOS SEMICUSTOM INTEGRATED CIRCUITS:	1987	JEDEC	0
1050	MO-059-B	Registration - Small Outline (SO) Package Family 8.4 mm (.330 inch) Body Width (Plastic) with Increased Lead Thickness to 11.8 mil max. Item 11.11-214.	1987	JEDEC	0
1051	JESD14	SEMICONDUCTOR POWER CONTROL MODULES:	1986	JEDEC	0
1052	JESD12-2	ADDENDUM No. 2 to JESD12 - STANDARD FOR CELL-BASED INTEGRATED CIRCUIT BENCHMARK SET:	1986	JEDEC	0
1053	JESD12-3	ADDENDUM No. 3 to JESD12 - CMOS GATE ARRAY MACROCELL STANDARD:	1986	JEDEC	0
1054	JESD236-C	COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES	1986	JEDEC	0
1055	JESD7-A	STANDARD FOR DESCRIPTION OF 54/74HCXXXX AND 54/74HCTXXXX HIGH SPEED CMOS DEVICES:	1986	JEDEC	0
1056	JESD24	POWER MOSFETS:	1985	JEDEC	0
1057	JESD12	SEMICUSTOM INTEGRATED CIRCUITS (FORMERLY PUBLISHED AS STANDARD FOR GATE ARRAY BENCHMARK SET):	1985	JEDEC	0
1058	DO-204B-D	Registration - Lead Mounted Family (Round Lead Axial). Item 78, 73, 128.	1985	JEDEC	0
1059	JESD11	CHIP CARRIER PINOUTS STANDARDIZED FOR CMOS 4000, HC AND HCT SERIES OF LOGIC CIRCUITS:	1984	JEDEC	0
1060	JESD482-A	LIST OF PREFERRED VALUES FOR USE ON VARIOUS TYPES OF SMALL SIGNAL AND REGULATOR DIODES	1984	JEDEC	0
1061	JEP75	LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A.	1984	JEDEC	0
1062	JEP90	THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986. See JESD531, April 2002.	1983	JEDEC	0
1063	JESD4	DEFINITION OF EXTERNAL CLEARANCE AND CREEPAGE DISTANCES OF DISCRETE SEMICONDUCTOR PACKAGES FOR THYRISTORS AND RECTIFIER DIODES:	1983	JEDEC	0
1064	MO-001-F	Registration - Dual in-line Family. 7.62 mm Row Spacing. Variations: AJ-AM.	1983	JEDEC	0
1065	TO-226-G	Registration - Header Family Flat Index.	1983	JEDEC	0
1066	JESD370B	DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES:	1982	JEDEC	0
1067	JESD5	MEASUREMENT OF TEMPERATURE COEFFICIENT OF VOLTAGE REGULATOR DIODES:	1982	JEDEC	0
1068	JESD24- 7	ADDENDUM No. 7 to JESD24 - COMMUTATING DIODE SAFE OPERATING AREA TEST PROCEDURE FOR MEASURING dv/dt DURING REVERSE RECOVERY OF POWER TRANSISTORS:	1982	JEDEC	0
1069	JESD2	DIGITAL BIPOLAR LOGIC PINOUTS FOR CHIP CARRIERS:	1982	JEDEC	0
1070	JESD1	LEADLESS CHIP CARRIER PINOUTS STANDARDIZED FOR LINEARS:	1982	JEDEC	0
1071	JESD23	TEST METHODS AND CHARACTER DESIGNATION FOR LIQUID CRYSTAL DEVICES:	1982	JEDEC	0
1072	CO-006-A	Registration - Magazine, Type A, B and D, 68 Pin Leadless Ceramic Chip Carrier.	1982	JEDEC	0
1073	EIA318-1	ADDENDUM No. 1 to EIA-318 - CHARACTERIZATION OF A REVERSE TEST FIXTURE: SUPERSEDED BY EIA-318-B, July 1996.	1981	JEDEC	0
1074	JESD311A	MEASUREMENT OF TRANSISTOR NOISE FIGURE AT MF, HF, AND VHF	1981	JEDEC	0
1075	JESD381-A	METHOD OF DIODE Q MEASUREMENT:	1981	JEDEC	0
1076	JESD390A	STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS, Reaffirmed September 2003. RESCINDED October 2008	1981	JEDEC	0
1077	EIA308-A	PREPARATION OF OUTLINE DRAWINGS OF SOLID-STATE PRODUCTS FOR JEDEC TYPE REGISTRATION, RESCINDED May 2009	1981	JEDEC	0
1078	JESD471	SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES	1980	JEDEC	0
1079	JESD419-A	STANDARD LIST OF VALUES TO BE USED IN SEMICONDUCTOR DEVICE SPECIFICATIONS AND REGISTRATION FORMAT:	1980	JEDEC	0
1080	JESD13-B	STANDARD SPECIFICATION FOR DESCRIPTION OF B SERIES CMOS DEVICES:	1980	JEDEC	0

1081	EIA397-1	ADDENDUM No. 1 TO EIA-397:	1980	JEDEC	0
1082	DG-4.2	Design Requirements - General Requirements	1980	JEDEC	0
1083	CO-005-A	Registration - Magazine for Dual-In-Line Product (DIP), 7.62, 10.16, 15.24 mm Row Spacing. Variations AA-AF.	1979	JEDEC	0
1084	JEP100	TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.	1979	JEDEC	0
1085	TO-237-B	Registration - Header Family, Flat Index. See TO-226AA	1979	JEDEC	0
1086	CO-001-B	Registration - Magazine Family, Dual-In-Line (DIP), 7.620 mm Row Spacing. Variations AA-AB.	1978	JEDEC	0
1087	CO-002-B	Registration - TO-220 Magazine.	1978	JEDEC	0
1088	CO-003-B	Registration - Magazine Family, Dual-In-Line (DIP), 7.620 mm Row Spacing. Variation AA.	1978	JEDEC	0
1089	CO-004-B	Registration - Square Magazine for Dual-In-Line Product (DIP). Variation AA	1978	JEDEC	0
1090	JEP99	GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.	1977	JEDEC	0
1091	JESD10	LOW FREQUENCY POWER TRANSISTORS:	1976	JEDEC	0
1092	JESD435	STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:	1976	JEDEC	0
1093	JESD313-B	THERMAL RESISTANCE MEASUREMENTS OF CONDUCTION COOLED POWER TRANSISTORS:	1975	JEDEC	0
1094	JEP69-B	PREFERRED LEAD CONFIGURATION FOR FIELD-EFFECT TRANSISTORS:	1973	JEDEC	0
1095	JESD25	MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:	1972	JEDEC	0
1096	JESD398	MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE:	1972	JEDEC	0
1097	EIA397	RECOMMENDED STANDARD FOR THYRISTORS:	1972	JEDEC	0
1098	JESD371	THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO:	1970	JEDEC	0
1099	JESD372	THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR ADMITTANCE PARAMETERS:	1970	JEDEC	0
1100	JEB5-A	METHODS OF MEASUREMENT FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS:	1970	JEDEC	0
1101	JEP78	RELATIVE SPECTRAL RESPONSE CURVES FOR SEMICONDUCTOR INFRARED DETECTORS:	1969	JEDEC	0
1102	JEP79	LIFE TEST METHODS FOR PHOTOCONDUCTIVE CELLS:	1969	JEDEC	0
1103	EIA365	PERFORMANCE TEST PROCEDURE FOR SOLAR CELLS AND CALIBRATION PROCEDURE FOR SOLAR CELL STANDARDS FOR SPACE VEHICLE SERVICE:	1969	JEDEC	0
1104	MO-213-A	Registration - Horizontal Staggered Surface Mount Package 0.40 mm Lead Pitch. Item 11.11-514.	1969	JEDEC	0
1105	JESD353	THE MEASUREMENT OF TRANSISTOR NOISE FIGURE AT FREQUENCIES UP TO 20 kHz BY SINUSOIDAL SIGNAL-GENERATOR METHOD:	1968	JEDEC	0
1106	JESD354	THE MEASUREMENT OF TRANSISTOR EQUIVALENT NOISE VOLTAGE AND EQUIVALENT NOISE CURRENT AT FREQUENCIES OF UP TO 20 kHz:	1968	JEDEC	0
1107	JESD340	STANDARD FOR THE MEASUREMENT OF CRE:	1967	JEDEC	0
1108	JESD6	MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE:	1967	JEDEC	0
1109	JEP65	TEST PROCEDURES FOR VERIFICATION OF MAXIMUM RATINGS OF POWER TRANSISTORS:	1967	JEDEC	0
1110	EIA323	AIR-CONVECTION-COOLED, LIFE TEST ENVIRONMENT FOR LEAD-MOUNTED SEMICONDUCTOR DEVICES:	1966	JEDEC	0
1111	JESD302	RANGES AND CONDITIONS FOR SPECIFYING BETA FOR LOW POWER, AUDIO FREQUENCY TRANSISTORS FOR ENTERTAINMENT SERVICE:	1965	JEDEC	0
1112	JESD306	MEASUREMENT OF SMALL SIGNAL HF, VHF, AND UHF POWER GAIN OF TRANSISTORS:	1965	JEDEC	0
1113	JESD307	VOLTAGE REGULATOR DIODE NOISE VOLTAGE MEASUREMENT:	1965	JEDEC	0
1114	JESD284-A	TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE	1963	JEDEC	0
1115	MPDRAM3.1	MPDRAM (Video RAM)	0	JEDEC	0

1116	CO-021-A	Registration - Plastic Magazine Family, Coinstack. Variations Variations AA-AC. Item 11.5-339.	0	JEDEC	0
1117	CO-022-A	Registration - Plastic Magazine Plug Family. Variations AA-AC. Item 11.5-340.	0	JEDEC	0
1118	CO-023-A	Registration - TapePak Plug Family, Coinstack Magazine. Variation AA-AC. Item 11.5-300.	0	JEDEC	0
1119	CO-025-A	Registration - MCR Plug Family, 36 mm, 46 mm and 56 mm Flat Plastic Tube Sizes, Magazine. Variations AA-AC. Item 11.5-351.	0	JEDEC	0
1120	CO-026-A	Registration - MCR Tube Family, 36 mm, 46 mm and 56 mm Flat Plastic Tube Sizes, Magazine. Variations AA-AC. Item 11.5-350.	0	JEDEC	0
1121	CO-027-B	Registration - Thin Tray for MQFP Packages (Removal of 5 Variations). Item 11.5-445.	0	JEDEC	0
1122	CO-028-B	Registration - Thick Matrix Tray for BGA. Item 11.5-435.	0	JEDEC	0
1123	CS-001-B	Standard - Metric Tape Automated Bonding (TAB) Magazine Family, 50, 100 Leads. Variations AA-AC. Replaces CO-017. Item 11.5-428S	0	JEDEC	0
1124	CS-006-A	Standard - Metric Tape Automated Bonding (TAB) Tape Carrier Family. (Supersedes CO-018). Item 11.11-353S	0	JEDEC	0
1125	CS-007-A	Standard - Thin Matrix Tray for TQFP.	0	JEDEC	0
1126	DO-200-D	Registration - Disc Type Family. Variations AA-AD.	0	JEDEC	0
1127	DO-200-E	Registration - Disc Type Family. Variation AE. Item 118.	0	JEDEC	0
1128	DO-203-B	Registration - Stud-Hex Base Family, Solid Terminals. Variations AA-AB. Ref. DO-4, DO-5.	0	JEDEC	0
1129	DO-205-C	Registration - Stud-Hex Base Family, Flexible Terminals. Item 11.10-231.	0	JEDEC	0
1130	DO-208-A	Registration - Press Fit Case Family, Single-End, Flanged, Axial Lead. Ref. DO-21.	0	JEDEC	0
1131	DO-209-A	Registration - Press Fit Case Family, Single-End, Solid Terminals. Ref. DO-24.	0	JEDEC	0
1132	DO-213-D	Registration - Update of AC Configuration - Leadless Family. Item 11.10-240.	0	JEDEC	0
1133	DO-216-A	Registration - Gullwing Plastic Surface Mount. Item 11.10-359.	0	JEDEC	0
1134	DO-217-A	Registration - Ceramic Button Rectifier, No Leads, 3 Variations. Item 11.10-362.	0	JEDEC	0
1135	GS-001	Registration - Dual-In-Line Gauge, 4 Lead, Axial Type.	0	JEDEC	0
1136	GS-002	Registration - Dual-In-Line Gauge, 4 Lead, Axial Type.	0	JEDEC	0
1137	MO-002-B	Registration - Header Family .200 inch Pin Circle. Variations AA-AH. Ref. TO-76, TO-73, TO-74, TO-75, TO-77, TO-78, TO-79.	0	JEDEC	0
1138	MO-002-C	Registration - Header Family .200 inch Pin Circle. Variations AJ-AL. Ref. TO-80, TO-99.	0	JEDEC	0
1139	MO-005-B	Registration - Grid Array Family, 3.18 mm Pitch. Variations AA-AB.	0	JEDEC	0
1140	MO-006-C	Registration - Header Family, 5.842 mm Pin Circle. Variations AA-AD. Ref. TO-96, TO-97, TO-100.	0	JEDEC	0
1141	MO-006-D	Registration - Header Family, 5.842 mm Pin Circle. Variations AE-AH. Ref. TO-101.	0	JEDEC	0
1142	MO-014-C	Registration - Flange-Mounted Family, Axial Lead, 7.62/8.25 Pin Circle.	0	JEDEC	0
1143	MO-015-G	Registration - Dual-In-Line Plastic (DIP) Family, .600 inch Row Spacing. Item 11.11-293.	0	JEDEC	0
1144	MO-016-D	Registration - Dual-In-Line Plastic (DIP) Family, .900 inch Row Spacing. Addition of 50, 52 and 64 Leads. Item 11.11-276	0	JEDEC	0
1145	MO-017-B	Registration - Axial Quad Family 2.54 mm Pitch. Variation AA-AC.	0	JEDEC	0
1146	MO-018-C	Registration - Flatpack Family, 10.16 mm Width, .89 Pitch. Variation AA.	0	JEDEC	0
1147	MO-020-C	Registration - Flatpack Family, 12.70 mm Width, 1.27 Pitch. Variations AA-AD.	0	JEDEC	0
1148	MO-021-C	Registration - Flatpack Family, 15.24 mm Width, 1.27 Pitch. Variations AA-AC.	0	JEDEC	0
1149	MO-022-A	Registration - Flatpack Family .700 Width, .050 Pitch. Variation AE. Item 11.3-077	0	JEDEC	0
1150	MO-022-D	Registration - Flatpack Family, 17.780 mm Width, 1.27 Pitch. Variations AA-AD. Item	0	JEDEC	0
1151	MO-023-C	Registration - Flatpack Family, 22.86 mm Width, 1.27 Pitch. Variations AA-AB.	0	JEDEC	0
1152	MO-024-C	Registration - Dual-In-Line (DIP) Family, 12.70 mm Row Spacing, Variations AA-AB.	0	JEDEC	0
1153	MO-025-B	Registration - Flange-Mounted Family, Axial Lead, 12.70 Pin Circle.	0	JEDEC	0

1154	MO-027-A	Registration - Leadless Flatpack Family, 1.27 mm Terminal Spacing. Item 11.3-055.	0	JEDEC	0
1155	MO-028-B	Registration - Dual-In-Line (DIP) Family, 5.08 mm Row Spacing. 10 Pin. Item 11.3-027.	0	JEDEC	0
1156	MO-029-B	Registration - Quad-In-Line (QUIP) Family, 5.08/10.16 mm Row Spacing. Variation AA-AB. Item 11.3-034/035	0	JEDEC	0
1157	MO-030-B	Registration - Quad-In-Line (QUIP) Family, 19.05/23.50 mm Row Spacing. Item 11.3-037.	0	JEDEC	0
1158	MO-031-D	Registration - Quad-In-Line (QUIP) Family, 5.08/10.16 mm Row Spacing. Variations AA-AB. Item 11.3-032/033.	0	JEDEC	0
1159	MO-032-C	Registration - Flatpack Family 16.64 mm Width, 1.27 Pitch. Variations AA-AF. Item 11.3-064.	0	JEDEC	0
1160	MO-033-B	Registration - Quad In Line (QUIP) Family 17.78/ 22.86 mm Row Spacing. Item 11.10-	0	JEDEC	0
1161	MO-034-C	Registration - 64 Lead Quad In-Line Package (QUIP) Family .750/.925 inch Row Spacing. Addition of Variation AD. Item 11.11-278.	0	JEDEC	0
1162	MO-035-A	Registration - Single-In-Line (SIP) Family. Item 11.3-79.	0	JEDEC	0
1163	MO-036-B	Registration - Rescission of MO-036 Variations AB-AE, Update of Variation AA to a .288 inch Wide Body. Item 11.10-384/388.	0	JEDEC	0
1164	MO-037-A	Registration - Ceramic Side Leaded Dual-In-Line (DIP) Family, 10.16 mm Row Spacing. Item 11.10-375S.	0	JEDEC	0
1165	MO-038-A	Registration - Ceramic Side Leaded Dual-In-Line (DIP) Family, .600 Row Spacing.	0	JEDEC	0
1166	MO-039-A	Registration - Ceramic Side Leaded Dual-In-Line (DIP) Family, .900 Row Spacing.	0	JEDEC	0
1167	MO-040-C	Registration - Power Module. Recission of Variation AB.	0	JEDEC	0
1168	MO-041-C	Registration - .050 inch Center Leadless Rectangular Chip Carrier Type E. Variations AA-AF. Item 11.10-350.	0	JEDEC	0
1169	MO-042-A	Registration - .050 inch Center Leadless Rectangular Chip Carrier Type F. Item 11.3-101.	0	JEDEC	0
1170	MO-043-A	Registration - Dual-In-Line Package 19.05 mm Row Spacing. Item 11.11-143.	0	JEDEC	0
1171	MO-044-A	Registration - Leaded Ceramic Chip Carrier .050 inch Center, 68 and 84 Terminals. Item 11.11-138.	0	JEDEC	0
1172	MO-045-A	Registration - Single-In-Line Power Module. Item 11.3-128.	0	JEDEC	0
1173	MO-046-B	Registration - Small Outline (SO) Package Peripheral Terminals 5.30 mm (.200 inch) Wide Body. Item 11.3-147.	0	JEDEC	0
1174	MO-047-B	Registration - Plastic Chip Carrier (PCC) Family .050 inch Lead Spacing, Square. Item 11.11-242.	0	JEDEC	0
1175	MO-048-A	Registration - Plastic Flange-Mounted Header Family Multilead Registration. Item 11.11-205.	0	JEDEC	0
1176	MO-054-A	Registration - Zig-Zag In-Line Package (ZIP) Family, 2.54 mm Row Spacing, 16 Pin. Item 11.11-133.	0	JEDEC	0
1177	MO-055-A	Registration - Ceramic Single-In-Line Package (SIP) Family. Item 11.10-207.	0	JEDEC	0
1178	MO-056-A	Registration - Ceramic .025 inch Center Chip Carrier. Item 11.10-124.	0	JEDEC	0
1179	MO-057-A	Registration - Ceramic .020 inch Center Chip Carrier. Item 11.10-124	0	JEDEC	0
1180	MO-060-B	Registration - .040 inch, 132 Pin Quad Flatpack. Item 11.10-278.	0	JEDEC	0
1181	MO-062-A	Registration - 148 Pin Leadless Ceramic Chip Carrier .025 inch mil Pitch. Item 11.10-235.	0	JEDEC	0
1182	MO-063-A	Registration - Plastic Small Outline J-Lead (SOJ) .350 inch Wide Body, .050 inch Lead Spacing, 26/20 Pin. Item 11.11-210..	0	JEDEC	0
1183	MO-064-C	Registration - 30 Pin Circuit Pluggable Single-In-Line Package (SIP) TABs on .100 inch Centers. Addition of Variation AE. Item 11.14-009.	0	JEDEC	0
1184	MO-065-A	Registration - Plastic Small Outline J-Lead (SOJ) .300 inch Wide Body Family, 0.050 Lead Spacing, 24 and 26 Pins. Item 11.11-216..	0	JEDEC	0
1185	MO-066-C	Registration - .100 inch Center Ceramic Pin Grid Array Family (Small Outline). Item 11.10-122.	0	JEDEC	0
1186	MO-067-B	Registration - .100 inch Center Ceramic Pin Grid Array Family (Large Outline). Item 11.10-122.	0	JEDEC	0
1187	MO-068-B	Registration - Edge Clip SIP Module Family, .100 Row Centers. Addition of Variation AF. Item 11.14-004.	0	JEDEC	0
1188	MO-069-B	Registration - Plastic Quad Flatpack .025 inch Lead Spacing (Gullwing). Item 11.11-285.	0	JEDEC	0
1189	MO-070-A	Registration - Rectangular Ceramic .375 inch Nominal Width Flatpack Family. Item 11.10-233.	0	JEDEC	0
1190	MO-071-B	Registration - Plastic Thin Lead Package Family Square (Gullwing). Item 11.11-239/240.	0	JEDEC	0

1191	MO-072-B	Registration - 40 Lead Zig-Zag In-Line Package Family (ZIP) 0.500 inch Max Seated Height. Addition of Variation AE. Item 11.11-284.	0	JEDEC	0
1192	MO-073-A	Registration - Ceramic Top Brazed Dual-In-Line Package (DIP) Family .900(22.86) Row Spacing. Item 11.10-206.	0	JEDEC	0
1193	MO-074-A	Registration - Ceramic Bottom Brazed Dual-In-Line Package (DIP) Family .900(22.86) Row Spacing. Item 11.10-206.	0	JEDEC	0
1194	MO-075-A	Registration - .050 inch Center Non-Hermetic Leadless Chip Carrier Quad Series, Square. Item 11.11-221.	0	JEDEC	0
1195	MO-076-A	Registration - .050 inch Center Non-Hermetic Leadless Chip Carrier SO Series, Rectangular. Item 11.11-222.	0	JEDEC	0
1196	MO-077-D	Registration - Small Outline J-Lead (SOJ) .300 inch Body, .050 inch Lead Spacing. Addition of a 42 Lead Package. Item 11.11-400.	0	JEDEC	0
1197	MO-078-A	Registration - Hermetic Flange-Mounted Header Family, Peripheral Leads, .100 mil Pitch, 5 Leads. Item 11.10-249.	0	JEDEC	0
1198	MO-079-A	Registration - Center Hermetic Flanged Family with Peripheral Leads .125 Pitch. Item 11.10-217.	0	JEDEC	0
1199	MO-080-A	Registration - ZIP Module Family 0.050 inch Pin Center, 0.100 inch Row Center, 23, 25, 26 and 28 Leads. Variations AA-AB. Item 11.11-218.	0	JEDEC	0
1200	MO-081-A	Registration - Ceramic Quadpack Family .050 inch Pitch, 68 Terminals, Type Q. Item 11.10-224.	0	JEDEC	0
1201	MO-082-A	Registration - Ceramic Quad Flat Pack .025 inch Lead Spacing (Gullwing). Item 11.10-246.	0	JEDEC	0
1202	MO-083-A	Registration - .100 inch Center Plastic Pin Grid Array Family (Nonhermetic). Item 11.11-243.	0	JEDEC	0
1203	MO-084-A	Registration - Ceramic Quad Flat Pack .050 inch Lead Spacing (Gullwing). Item 11.10-255.	0	JEDEC	0
1204	MO-085-A	Registration - .040 inch Center Rectangular Leadless Package (Staggered Terminals). Item 11.10-165.D270	0	JEDEC	0
1205	MO-086-B	Registration - Low Profile Plastic Quad Flatpack Family .025 Lead Spacing (Gullwing). Item 11.11-267.	0	JEDEC	0
1206	MO-087-B	Registration - J-Lead Ceramic CERQUAD Package Family .050 inch Pitch. Item 11.10-286.	0	JEDEC	0
1207	MO-088-A	Registration - Small Outline J-Lead (SOJ) Family Peripheral terminals, 7.50 (.300 inch) Wide Body (MS-113 Body). Variations AA-AF. Item 11.11-206.	0	JEDEC	0
1208	MO-089-A	Registration - Plastic Quad Flatpack Family, .050 inch Lead Spacing (Gullwing). Item 11.11-231.	0	JEDEC	0
1209	MO-090-B	Registration - Top Brazed Ceramic Quadpack Family .025 inch Pitch, 100 Leads. Variations AA-AF. Item 11.10-264.	0	JEDEC	0
1210	MO-091-A	Registration - Plastic Small Outline J-Lead (SOJ) .350 Wide Body Family, 28 Pins. Item 11.11-232.	0	JEDEC	0
1211	MO-092-A	Registration - 6.35 mm Width Ceramic Flatpack (CERPAKS). Item 11.10-270.	0	JEDEC	0
1212	MO-093-A	Registration - Plastic Single Flange-Mounted Header, 5-Lead. Item 11.10-259.	0	JEDEC	0
1213	MO-094-C	Registration - TapePak Molded Carrier Ring Family. Zero Degree Minimum Lead Bend. Item 11.11-328.	0	JEDEC	0
1214	MO-095-A	Registration - Dual-In-Line (Wide Body) Plastic Family .300 inch Row Spacing. Item 11.11-262/266.	0	JEDEC	0
1215	MO-096-A	Registration - Flange-Mounted Header, 7-Lead. Item 11.10-260.	0	JEDEC	0
1216	MO-097-A	Registration - Flange-Mounted Family Axial Lead .600 inch Pin Circle. Item 11.10-273.	0	JEDEC	0
1217	MO-098-A	Registration - Bottom Brazed Lead Flatpack Family (10, 14, 16 and 18 Leads). Item 11.10-280.	0	JEDEC	0
1218	MO-099-A	Registration - Small Outline (SO) Family Peripheral Terminals .440 inch Body Width (Plastic), 28 and 32 Leads with 0.050 inch Lead Spacing. Item 11.11-217.	0	JEDEC	0
1219	MO-100-A	Registration - Multilayer Ceramic Quad Flatpack .020 Spacing Gullwing (256 leads). Item 11.10-271	0	JEDEC	0
1220	MO-103-B	Registration - Dual-In-Line Cerdip Family .600 inch Row Spacing. Item 11.10-383	0	JEDEC	0
1221	MO-104-A	Registration - Ceramic Quad (CERQUAD) Flatpack, 0.025 inch Pitch, Gullwing Leadform (132 Leads). Item 11.10-283.	0	JEDEC	0
1222	MO-105-A	Registration - Thin Small Outline J-Lead (TSOJ) .300 inch Body, 0.050 inch Lead Pitch. Item 11.11-272.	0	JEDEC	0
1223	MO-106-A	Registration - Flatpack Family for High Speed ECL Memory Devices, .535 inch Length, .030 inch Pitch (22, 24 and 28 Pins). Item 11.10-281.	0	JEDEC	0
1224	MO-107-A	Registration - Ceramic Multilayer Leaded Chip Carrier ,.050 inch Pitch, J-Bend Leadform, 20 mil min. Item 11.10-284.	0	JEDEC	0
1225	MO-108-C	Registration - Metric Plastic Quad Flatpack, 1.0, 0.8, 0.65 mm. Item 11.11-449.	0	JEDEC	0
1226	MO-109-B	Registration - TapePak Molded Carrier Ring Family, Zero Degree Minimum Lead Bend. Item 11.11-329.	0	JEDEC	0
1227	MO-110-A	Registration - Round Lead, inchJ inch Form Square Body, .050 inch Pitch Center Ceramic Chip Carrier. Item 11.10-292.	0	JEDEC	0

1228	MO-111-A	Registration - Family of Round Leads, .050 inch Pitch, Gullwing Leadform, Center Ceramic Chip Carrier. Item 11.10-293.	0	JEDEC	0
1229	MO-112-B	Registration - Metric Quad Flatpack Family (Plastic) 3.9 mm Footprint. Item 11.11-422.	0	JEDEC	0
1230	MO-113-D	Registration - Ceramic Quadpack Family 0.025 inch Lead Spacing With Ceramic Nonconductive Tie Bar. Item 11.10-369.	0	JEDEC	0
1231	MO-114-C	Registration - 28 mm Glass Sealed Ceramic Quad Flatapack Family Gullwing Leadform 0.65, 0.80 mm Pitch. Item 11.10-357	0	JEDEC	0
1232	MO-115-A	Registration - Bottom-Brazed Lead Flatpack Family, 32 Leads, .480 inch Wide . Item 11.10-302.	0	JEDEC	0
1233	MO-116-B	Registration - 72 Circuit Pluggable Single-In-Line Memory Module (SIMM) with Tabs on .050 inch Centers. Item 11.14-023S.	0	JEDEC	0
1234	MO-117-A	Registration - Small Outline Plastic Package 12 mm Wide Body with Gullwing, 0.80 mm Lead Spacing. Item 11.11-289.	0	JEDEC	0
1235	MO-118-B	Registration - Shrink Small Outline Package Family, 0.25 inch Lead Pitch .300 inch Wide Body. Item 11.11-309.	0	JEDEC	0
1236	MO-119-B	Registration - Plastic Small Outline (SO) Package Family With .300 inch Body Width. Item 11.11-298.	0	JEDEC	0
1237	MO-120-B	Registration - Plastic Small Outline (SO) Package Family With .350 inch Body Width. Item 11.11-300.	0	JEDEC	0
1238	MO-121-B	Registration - Plastic Small Outline (SO) Package Family. J-Lead, .330 inch Body Width. Item 11.11-301.	0	JEDEC	0
1239	MO-122-A	Registration - Thin Dual-In-Line Family, 14, 16, and 18 Leads .300 inch Row Spacing (Plastic). R-PDIP-T. Item 11.11-318.	0	JEDEC	0
1240	MO-123-A	Registration - Small Outline, 64 Leads, 12 mm Body, J-Lead, 0.80 mm Lead Spacing. Item 11.11-304.	0	JEDEC	0
1241	MO-124-B	Registration - Small Outline J-Lead (SOJ) 12.70 mm Body 1.27 mm Lead Spacing. Item 11.11-371.	0	JEDEC	0
1242	MO-125-A	Registration - Multilayer Ceramic Quad Flatpack .025 Spacing Gullwing (196 Leads). Item 11.10-303.	0	JEDEC	0
1243	MO-126-B	Registration - Leadless Small Outline Ceramic Chip Carrier, .400 inch Body, .050 inch Pitch. 28, 32, 26 Leads. Variations AA-AC. Item 11.10-318.	0	JEDEC	0
1244	MO-127-A	Registration - Power Dual-In-Line Package. Item 11.10-297.	0	JEDEC	0
1245	MO-128-C	Registration - Ceramic Staggered PGA 100 inch Centers (Large Outline). Variations AA-BQ. Item 11.10-365.	0	JEDEC	0
1246	MO-129-A	Registration - Top Brazed Ceramic Leaded Chip Carrier (.020 inch Lead Pitch) with Plastic Non-Conductive Tie Bar. Item 11.10-298.	0	JEDEC	0
1247	MO-130-A	Registration - Top Brazed Ceramic Leaded Chip Carrier (.015 inch Lead Pitch) with Plastic Non-Conductive Tie Bar. Item 11.10-299.	0	JEDEC	0
1248	MO-131-A	Registration - Top Brazed Ceramic Leaded Chip Carrier (.025 inch Lead Pitch) with Plastic Non-Conductive Tie Bar. Item 11.10-290.	0	JEDEC	0
1249	MO-132-B	Registration - TSOP I, 7.62 mm Body. Item 11.11-346.	0	JEDEC	0
1250	MO-135-C	Registration - Thin Small Outline Package (TSOP II) 12.70 mm Body Family. Item 11.11-358.	0	JEDEC	0
1251	MO-139-A	Registration - 16 Lead Flange-Mounted Ceramic Power Package. (Type 2), R-CDFM-T16. Item 11.10-311.	0	JEDEC	0
1252	MO-140-A	Registration - 18 Lead Flange-Mounted Ceramic Power Package. R-CDFM-T18. Item 11.10-312.	0	JEDEC	0
1253	MO-141-A	Registration - Vertical Surface Mount Package, 0.50 mm Lead Pitch, R-PSIP-X24. Item 11.11-319.	0	JEDEC	0
1254	MO-142-D	Registration - Thin Small Outline Package (Type I). S-PDSO-G/TSOP. Correction of the L min value from 0.05 mm to 0.50 mm. Item 11.1-583E	0	JEDEC	0
1255	MO-144-A	Registration - Leadless Small Outline Ceramic Chip Carrier, .350 inch Body, .050 inch Pitch. R-CDCC-N. Item 11.10-319.	0	JEDEC	0
1256	MO-145-A	Registration - .050 inch Center Ceramic Surface Mount Pin Grid Array (PGA) Family. S-CPGA-B/SMTPGA. Item 11.10-324.	0	JEDEC	0
1257	MO-146-A	Registration - Ceramic Flatpack Family .380 inch Width, .025 Pitch. R-GDFP-F. Item 11.10-320.	0	JEDEC	0
1258	MO-152-C	Registration - Plastic Shrink Small Outline Package (SSOP). R-PSDO-G/SSOP. Item 11.11-440.	0	JEDEC	0
1259	MO-154-C	Registration - Shrink Small Outline Package Family, 0.4mm and .5 mm Lead Pitch, SSOP 3.9 mm Body Width, Addition of 80 and 96 Pin Variations. Item 11.11-459.	0	JEDEC	0
1260	MO-155-A	Registration - Plastic Small Outline (SOP), 5-Lead. Item 11.11-364.	0	JEDEC	0
1261	MO-159-B	Registration - Ceramic CGA Rectangular. Item 11.10-371.	0	JEDEC	0

1262	MO-160-B	Registration - 72 Pin Dual-In-Lin Memory Module (DIMM) Family with 1.27 mm Contact Centers. Variations AA-CC. Addition of 84 Contact Variation. Item 11.14-017.	0	JEDEC	0
1263	MO-162-A	Registration - Plastic Flatpack/Heat Slug Package, 0.8 mm Pitch, 48 Leads. Item 11.11-370.	0	JEDEC	0
1264	MO-164-A	Registration - Plastic Shrink SO Package Family, 9.9 mm Wide Body, 36 and 70 Pins R-PDSO-G . Item 11.11-331	0	JEDEC	0
1265	MO-165-C	Registration - Plastic Small Outline J-Lead (SOJ), 10.15 mm Body Width, .8 mm pitch R-PDSO-J. Addition of 44 Pin Variation. Item 11.11-455	0	JEDEC	0
1266	MO-166-D	Registration - Plastic SO with Heat Slug, 20, 24, 30, 36 leads. Addition of a 44 lead (0.65 mm pitch) Plastic Heat Slug Package. Variations AA-AE. Item 11.11-551.	0	JEDEC	0
1267	MO-167-C	Registration - 128 Pin Dual-In-Line memory Module (DIMM) Family, 1.27 mm Lead Centers. Item 11.14-029.	0	JEDEC	0
1268	MO-168-A	Registration - Plastic Isolated Flange-Mounted Header Family. Variations AA-AB. Item 11.10-344.	0	JEDEC	0
1269	MO-170-A	Registration - 68 Pin (Type I), 68-Pin (Type II) and 88 Pin Memory Card. Item 11.14-010.	0	JEDEC	0
1270	MO-171-A	Registration - 88 Pin Memory Card. Item 11.14-012.	0	JEDEC	0
1271	MO-172-D	Registration - 112 & 200 Pin Dual-In-Line Memory Module (DIMM) Family, 1.27 mm Pitch. Item 11.14-041.	0	JEDEC	0
1272	MO-173-A	Registration - Thin Quad Flatpack Family with Integral Heat Spreader. Item 11.11-403.	0	JEDEC	0
1273	MO-174-A	Registration - Plastic Shrink Small Outline Package (SSOP), 70-pin .8 mm Pitch, 3.9 mm Wide Body. Addition of 0.4 mm Variation. Item 11.11-401.	0	JEDEC	0
1274	MO-175-A	Registration - 44 and 48 Pin Plastic SOP, 12.6 mm Body, 1.27 mm Pitch. Item 11.11-412.	0	JEDEC	0
1275	MO-176-A	Registration - Ceramic Zig Zag In-Line Family (2.54 mm Row Spacing). Item 11.10-353.	0	JEDEC	0
1276	MO-178-C	Registration - 5 Pin SOT, 6 and 8 lead. Variations AB and BA to SOT. Item 11.10-397.	0	JEDEC	0
1277	MO-179-A	Registration - 278 Pin Dual-In-Line Meory module (DIMM) Family with 1.00 Lead Centers. Item 11.14-021.	0	JEDEC	0
1278	MO-181-A	Registration - Plastic Metric Small Outline J-Lead (MSOJ) Package, 16 mm Wide Body, 40 Pin. R-PDSO-J/SOJ. Item 11.11-418.	0	JEDEC	0
1279	MO-182-C	Registration - Metric TSOP II, 16 mm Body Width, 40 and 62 Leads. Item 11.11-454.	0	JEDEC	0
1280	MO-183-A	Registration - TSOP I, 0.55 mm Pitch, 28 Leads. Item 11.11-426.	0	JEDEC	0
1281	MO-184-B	Registration - Small Outline Heat Slug Variation B: Addition of Longer Foot (L) Variations to SOP. Item 11.11-548.	0	JEDEC	0
1282	MO-185-A	Registration - 72 Pin Staggered Dual-Inline Module (SDIM) Family. Item 11.14-022.	0	JEDEC	0
1283	MO-186-C	Registration - Solid State Floppy Disk Card, 32Contact. Item 11.14-035. Editorial Correction of the TAB Clearance Dimension in Detail A from 0.01 mm to 0.10 mm. Item 11.14-035E.	0	JEDEC	0
1284	MO-188-B	Registration - Power PQFP with Heat Slug. Item 11.11-559.	0	JEDEC	0
1285	MO-189-A	Registration - Plastic QFP/Heat Slug (H-LQP/G) 2.00 mm Thick/2.00 mm Footprint. Item 11.11-451.	0	JEDEC	0
1286	MO-191-A	Registration - 160 Pin Dual-In-Line Memory Module (DIMM) Family, 1.27 mm Lead Centers. Item 11.14-027.	0	JEDEC	0
1287	MO-194-B	Registration - TSSOP/HSSOP, 0Plastic Thin Shrink Small Outline Package. 0.40 mm Lead Pitch. Item 11.11-492.	0	JEDEC	0
1288	MO-196-C	Registration - Plastic Ultra-Thin Small Outline, No Lead Package. Item 11.11-508.	0	JEDEC	0
1289	MO-197-B	Registration - Plastic Ultra-Thin Small Outline No-Lead Package 0.5mm Pitch. Item 11.11-498.	0	JEDEC	0
1290	MO-198-A	Registration - 3-Tier Family. PQFP-B. Item 11.11-473.	0	JEDEC	0
1291	MO-199-B	Registration - Low Profile Small Outline J-Lead Package (LSOJ). Addition of 66 Lead Variation. Item 11.11-512.	0	JEDEC	0
1292	MO-200-B	Registration - Small Outline J-Lead Package Assembly 2 High/4 High Stack. Item 11.11-513.	0	JEDEC	0
1293	MO-202-A	Registration - Verticle Zig-Zag Surface Mount Package, 0.40 mm Lead Pitch, Plastic ZIP Package. Item 11.11-496.	0	JEDEC	0
1294	MO-209-A	Registration - Plastic Thin Shrink Fine Pitch Small Outline No Lead (TFSON) Package. Item 11.11-507.	0	JEDEC	0
1295	MO-212-A	Registration - Rectangular Plastic Quad Flat Package, 1.0 mm Thick Body, 3.2 mm Footprint. Item 11.11-511.	0	JEDEC	0
1296	MO-218-A	Registration - Plastic Flange-Mounted Staggered Header Family, 7 & 9 Lead TO Style Package. Item 11.10-393	0	JEDEC	0
1297	MO-223-A	Registration - 5, 6, and 8 Lead Plastic Thin Shrink Small Outline Package (TSSOP) to Align with EIAJ Standard SC-88. Item 11.10-402.	0	JEDEC	0

1298	MS-001-D	Standard - Dual-In-Line Plastic Family .300 inch Row Spacing. R-PDIP-T. Item 11.11-271S	0	JEDEC	0
1299	MS-002-A	Standard - .050 inch Leadless Chip Carrier, Type A. Variations AA-AH.	0	JEDEC	0
1300	MS-003-A	Standard - .050 inch Leadless Chip Carrier, Type B. Variation BA-BH.	0	JEDEC	0
1301	MS-004-B	Standard - .050 inch Center Leadless Chip Carrier, Type C. Variations CA-CH. Item 11.10-237.	0	JEDEC	0
1302	MS-005-A	Standard - .050inch Center Leadless Chip Carrier, Type D. Variations DA-DH.	0	JEDEC	0
1303	MS-006-A	Standard - .050 inch Center Leaded Chip Carrier, 24 Terminal Leaded, Type A.	0	JEDEC	0
1304	MS-007-A	Standard - .050 inch Center Lead Chip Carrier, Type A. Variations AA-AH.	0	JEDEC	0
1305	MS-008-A	Standard - .050 inch Center Lead Chip Carrier, Type B. Variations BA-BH.	0	JEDEC	0
1306	MS-009-A	Standard - .040 inch Center Leadless Chip Carrier Packages. Variations AA-AJ.	0	JEDEC	0
1307	MS-010-C	Standard - Plastic DIP .400 inch Row Spacing, 28 and 32 Leads. Addition of Variations AC and AD. Item 11.11-306.	0	JEDEC	0
1308	MS-011-B	Standard - Plastic DIP .600 inch Row Spacing, 48 Lead. Addition of Variation AD. Item 11.4-238.	0	JEDEC	0
1309	MS-014-A	Standard - Single Layer Chip Carrier Family, .040 inch Terminal Spacing, Ceramic. Variations AA-AJ. Item 11.3-112.	0	JEDEC	0
1310	MS-015-A	Standard - Side Brazed Ceramic DIPs in .300 inch, .400 inch and .900 inch Center Line Row-to-Row Spacing. Item 11.10-272.	0	JEDEC	0
1311	MO-052-A	Replaced - See MS-016-A. (Plastic Chip Carrier (PCC) Family .050 inch Leadspacing, Rectangular).	0	JEDEC	0
1312	MS-017-B	Standard - Ceramic PGA .100 inch Pitch Cavity Down . Item 11.10-315.	0	JEDEC	0
1313	MS-018-A	Standard - Square Plastic Chip Carrier Family, 1.27 mm/.050 inch Pitch. Item 11.11-252S.	0	JEDEC	0
1314	MS-019-B	Standard - Dual-In-Line (Shrink .070 inch) Plastic Package Family .300 inch Row Spacing. R-PDIP-T. Item 11.11-290S.	0	JEDEC	0
1315	MS-020-B	Standard - Dual-In-Line (Shrink .070 inch) Plastic Package Family .600 inch Row Spacing. R-PDIP-T. Item 11.11-291S	0	JEDEC	0
1316	MS-021-A	Standard - Dual-In-Line (Shrink .070 inch) Plastic Package Family .750 inch Row Spacing. R-PDIP-T. Item 11.11-292S.	0	JEDEC	0
1317	MS-022-B	Standard - Metric Plastic Quad Flat Pack 1.0,0.8,0.65 mm. Item 11.11-450S.	0	JEDEC	0
1318	MS-023-A	Standard - Plastic SOJ, .300 inch Body, .050 inch Lead Spacing. Item 11.11-330S.	0	JEDEC	0
1319	MS-025-B	Standard - TSOP II, 7.62 mm Body. Change to the Max. Bend Radius and Foot Angle. Item 11.11-518S	0	JEDEC	0
1320	MO-061-A	Replaced - See MS-027-A. Item 11.11-404S.	0	JEDEC	0
1321	MS-028-C	Standard - Addition of Rectangular BGA Variations to BGA Family. Item 11.11-550s.	0	JEDEC	0
1322	MO-143-C	Replaced - See MS-029-A. Item 11.11-484S. (Fine Pitch QFP, 0.5, 0.4 mm Pitch. S-PQFP-G/FQFP).	0	JEDEC	0
1323	MO-058-B	Replaced - See MS-030-A. Item 11.10-374S. (Dual-In-Line CERDIP Family .300 inch Row Spacing. Item 11.10-385).	0	JEDEC	0
1324	MS-031-A	Standard - Ceramic Dual-In-Line (CDIP) Family, .400 inch Row Spacing. Item 11.10-375S.	0	JEDEC	0
1325	MS-032-A	Standard - Ceramic Dual-In-Line (CDIP) Family, .600 inch Row Spacing. Item 11.10-376S.	0	JEDEC	0
1326	MO-004-C	Replaced - See MS-033-A. Item 11.10-382S. (Flatpack Family, .300 Width, .050 Pitch. Variations AJ-AM. Item 11.10-391).	0	JEDEC	0
1327	SPP-001	Standard Practices and Procedures - Document Procedure.	0	JEDEC	0
1328	SPP-002	Standard Practices and Procedures - Pin #1 Mark Function and Location.	0	JEDEC	0
1329	SPP-004	Standard Practices and Procedures - Lead Finish and base Metal Specification.	0	JEDEC	0
1330	SPP-005	Standard Practices and Procedures - Pin #1 orientation for TAB Packages.	0	JEDEC	0
1331	SPP-006	Standard Practices and Procedures - Definition of DAMBAR Protrusion and Intrusion.	0	JEDEC	0
1332	SPP-007	Standard Practices and Procedures - Use of -PROPOSED- on Ballots.	0	JEDEC	0
1333	SPP-008	Standard Practices and Procedures - Gullwing Lead Dimensioning.	0	JEDEC	0
1334	SPP-009	Standard Practices and Procedures - Inclusion of Nominal Dimensions.	0	JEDEC	0
1335	SPP-011	Standard Practices and Procedures - J Lead; Dimensioning of Lead Contact Points.	0	JEDEC	0
1336	SPP-012	Standard Practices and Procedures - Pin #1 Mark and Lead-Numbering Convention for Dual-In-Line Packages with Standard and Reverse-Bend Lead Form.	0	JEDEC	0

1337	SPP-015	Standard Practices and Procedures - Requirements for Applying Material and Finish Specifications to Selected Mechanical Outlines.	0	JEDEC	0
1338	SPP-016	Standard Practices and Procedures - Inactivation and Rescission.	0	JEDEC	0
1339	SPP-018	Standard Practices and Procedures - Procedure for Making Editorial Corrections to Published Documents.	0	JEDEC	0
1340	TO-200-J	Registration - Disc Type Family. Variations AE-AF. Item 92-3/119.	0	JEDEC	0
1341	TO-202-F	Registration - Tape Automated Bonding (TAB) Mounted Family Peripheral Leads.	0	JEDEC	0
1342	TO-204-C	Registration - Flange-Mounted Header Family .430 inch Pin Spacing. Variations AA-AD. Ref. TO-3, TO-41.	0	JEDEC	0
1343	TO-205-E	Registration - Header Family, .200 Pin Circle. Variations AA-AG. Item 11.2-109.	0	JEDEC	0
1344	TO-206-B	Registration - Header Family, .100 Pin Circle. Variations AA-AG. Item 11.2-109.	0	JEDEC	0
1345	TO-208-C	Registration - Stud Hex Base Family, Solid Terminals. Variations AE-AG. Ref. TO-103.	0	JEDEC	0
1346	TO-209-A	Registration - Stud Hex Base Family, Flexible Leads. Variations AA-AE. Ref. TO-49, TO-93, TO-94, TO108, TO-118.	0	JEDEC	0
1347	TO-213-A	Registration - Flange-Mounted Header Family, .200 Pin Spacing. Variations AA-AC. Ref. TO-66, TO-123, TO-124	0	JEDEC	0
1348	TO-215-A	Registration - Coaxial package Outline. Item 269G.	0	JEDEC	0
1349	TO-216-A	Registration - Stud-Mounted Stripline Header Family. Item 270G	0	JEDEC	0
1350	TO-218-E	Registration - Flange-Mounted Header Family, Axial and Peripheral Leads. Variations AA-AD.	0	JEDEC	0
1351	TO-219-B	Registration - Flange-Mounted Header Family, Axial and Peripheral Leads. Variations AA-AB. Item 240-G.	0	JEDEC	0
1352	TO-236-H	Registration - Revision to 3 lead SOT Package, Header Family. Item 11.10-379	0	JEDEC	0
1353	TO-238-D	Registration - Flange-Mounted Header Family, Rectangular Body. Variations AA-AC. Item 11.2-80-64/81-60.	0	JEDEC	0
1354	TO-240-B	Registration - Terminal Strip Family Power Module. Variations AA-AB.	0	JEDEC	0
1355	TO-243-C	Registration - Header Family, Peripheral Terminal. Variations AA-AB. (SOT-89). Item 11.10-213.	0	JEDEC	0
1356	TO-244-B	Registration - Flange-Mounted Family, Rectangular Base. Variation AA-AB. Item 11.2-105.	0	JEDEC	0
1357	TO-250-A	Registration - Dual-In-Line (DIP) Family, .300 inch Row Spacing, 4 Lead. Item 120.	0	JEDEC	0
1358	TO-253-D	Registration - Revision to 4 Lead Small Outline Transistor (SOT). Item 11.10-380	0	JEDEC	0
1359	TO-254-A	Registration - Flange-Mounted Header Family, Peripheral Terminals. Item 11.10-229	0	JEDEC	0
1360	TO-256-A	Registration - Flat Mounted Transistor. Item 11.10-245.	0	JEDEC	0
1361	TO-257-C	Registration - Revision - Flange Mounted Header Family (Peripheral Terminals). Item 11.10-361.	0	JEDEC	0
1362	TO-258-A	Registration - Hermetic Flange-Mounted Header Family, Peripheral Leads, .200 inch Wide, 5.08 Spacing, 3 Leads. Item 11.10-251.	0	JEDEC	0
1363	TO-259-B	Registration - Addition of Variation AB to Flange-Mounted Header Family. Item 11.10-307.	0	JEDEC	0
1364	TO-260-A	Registration - Ceramic Header Axial 3-Lead.	0	JEDEC	0
1365	TO-262-A	Registration - Flange-Mounted Header Family, Straight Leads, Similar to TO-220. Item 11.10-288	0	JEDEC	0
1366	TO-264-B	Registration - Flange-Mounted Header Family, 3 Lead, Peripheral Leaded Package. Item 11.10-.	0	JEDEC	0
1367	TO-265-A	Registration - 3 Lead Flange-Mounted Ceramic Power Package.R-CSFM-T3. Item 11.10-309.	0	JEDEC	0
1368	TO-266-A	Registration - Opto Family, Insertion Mount, Peripheral Terminals. Item 11.10-336.	0	JEDEC	0
1369	TO-267-A	Registrtaion - Hermetic Flange-Mounted Header Family, Peripheral Terminals, 3 Lead, 5.0 Spacing. R-MSFM-X3. Item 11.10-349.	0	JEDEC	0
1370	TO-268-A	Registration - Surface Mounted Header Family, Peripheral Terminals. R-PSFM-G2. Item 11.10-352.	0	JEDEC	0
1371	TO-269-A	Registration - 4 Lead Small Outline Package (SOP). Item 11.10-358	0	JEDEC	0
1372	TO-271-A	Registration - 4 Lead Quad Flat Pack (QFP).	0	JEDEC	0
1373	TO-274-A	Registration - 3 Lead Plastic Flange-Mounted Package. Item 11.10-401	0	JEDEC	0
1374	TS-001-A	Standard - Plastic Single-in-Line Flange-Mounted, 5 Leads. PSFM. Item 11.10-220.	0	JEDEC	0
1375	TS-002-A	Standard - Header Family, Insertion Mount, Peripheral Terminals. Item 11.10-322S	0	JEDEC	0

1376	TS-003-B	Standard - Header Family, Surface Mounted, Peripheral Terminals. R-PSFM-G2. Item 11.10-323S.	0	JEDEC	0
1377	TS-004-A	Standard - Flange-Mounted Header Family. R-PSFM-F3. Item 11.10-326S.	0	JEDEC	0
1378	TS-005-A	Standard - Surface Mounted Header Family, 2 Leads, Peripheral Terminals. R-PSFM-G. Item 11.10-327S.	0	JEDEC	0
1379	UO-017-A	Registration - Tape Automated Bonding (TAB) Package, 10, 15 and 20 mil Pitch Uncased Outline. Item 11.4-235/236/237.	0	JEDEC	0
1380	UO-018-B	Registration - Metric Super Format Tape Automated Bonding (TAB) Package Family.	0	JEDEC	0
1381	US-001-B	Standard - Tape Automated Bonding (TAB) Package Family. S-PQUC-X/TAB.	0	JEDEC	0

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